

# Photon counting imaging: the DigitalAPD

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## ABSTRACT

Geiger Mode avalanche photodiodes offer single photon detection, however, conventional biasing and processing circuitry make arrays impractical to implement. A novel photon counting concept is proposed which greatly simplifies the circuitry required for each device, giving the potential for large, single photon sensitive, imaging arrays. This is known as the DigitalAPD. The DigitalAPD treats each device as a capacitor. During a write, the capacitor is periodically charged to photon counting mode and then left open circuit. The arrival of photons causes the charge to be lost and this is later detected during a read phase. Arrays of these devices have been successfully fabricated and a read out architecture, employing well known memory addressing and scanning techniques to achieve fast frame rates with a minimum of circuitry, has been developed. A discrete prototype has been built to demonstrate the DigitalAPD with a 4x4 array. Line rates of up to 5MHz have been observed using discrete electronics. The frame burst can be transferred to a computer where the arrival of single photons at any of the 16 locations can be examined, frame by frame. The DigitalAPD concept is highly scalable and is soon to be extended to a fully integrated implementation for use with larger 32x32 and 100x100 APD arrays.

**Keywords:** Geiger Mode avalanche photodiodes, Photon Counting, APD, DigitalAPD

## 1. INTRODUCTION

### 1.1 Geiger Mode APDs

Geiger mode avalanche photodiodes (APDs) offer photon counting solutions in a wide range of application areas such as biosensors<sup>1,2</sup>, quantum cryptography<sup>3</sup> and medical diagnostics<sup>4</sup>. Shallow junction Geiger-mode APD technology provide a revolutionary alternative to the PMT Photomultiplier Tube, the existing standard for photon counting applications, offering advantages in terms of volume production, cost, size, operating voltage and robustness. The Geiger mode APD is manufactured in a CMOS compatible process that enables arrays of such devices to be manufactured.

The operation of Geiger mode APDs is in three phases. The device is placed in reverse bias typically at 5V-10V over the reverse breakdown voltage. When a photon hits the active area of the device a photoelectron is generated where thermally generated carriers diffuse to the depletion region causing a current flow through the device. The large current flow, known as avalanche breakdown, needs to be quenched to prevent damage to the device. A simple way to achieve this is to use a resistor in series with the APD to passively quench<sup>5</sup>. When current starts to flow the voltage increases across the resistor and thus reduces the bias across the APD to below the breakdown. When the current dissipates the voltage across the APD is reset and the device returns to Geiger mode. The output of the Geiger mode APD is therefore a series of current pulses corresponding to the arrival times of photons. These pulses can be sensed by using a lower valued resistor in line and a small capacitor in parallel with the quench resistor to output a workable voltage to a comparator that squares the pulses by comparison with a reference voltage (Fig 1). The disadvantage of passive quenching however is that maximum count rates are limited to the hundreds of kHz region by the RC time constants of the devices. Active quenching<sup>6</sup> circuitry (Fig 2) can be used to improve count rates to the order of 10MHz but with the cost of additional timing delay and discrete circuitry and the requirement of 10-15V quenching voltages.

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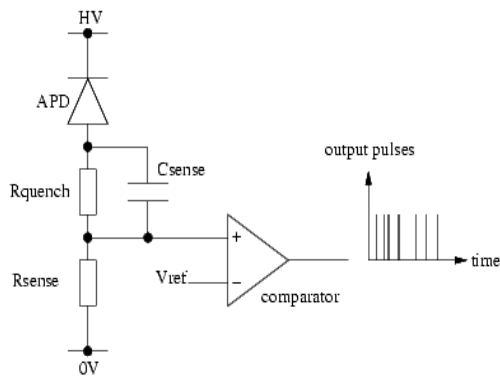


Figure 1: Passive quench circuitry

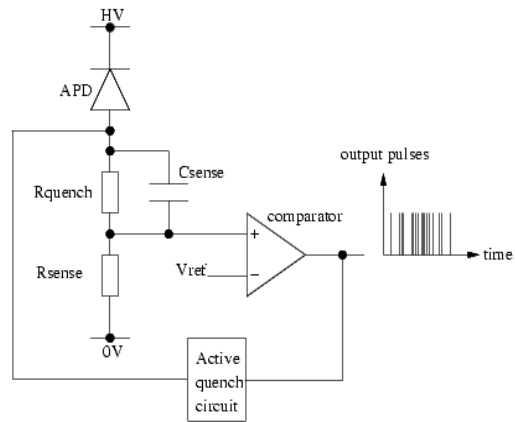


Figure 2: Active quench circuitry

## 1.2 Motivation for the DigitalAPD

Typically active quench circuitry takes a considerable area on PCBs or silicon and this has impeded the commercial advance of Geiger mode APD arrays. Early research attempts to integrate arrays of photodiodes typically suffered from afterpulsing, noise and poor quantum efficiency<sup>7</sup>. The SPADA<sup>8</sup> (single-photon avalanche diode array) has shown improvements in these specifications, however each APD connection is individually accessed to the edge of the array making the average silicon area for an APD quite large. Therefore big arrays would be expensive. Quench circuitry has been integrated within the silicon array<sup>9</sup> but, in order to eliminate crosstalk, the pitch of these devices is still quite large compared to active area and the n-well process used<sup>10</sup> led to low quantum efficiency. MIT Lincoln Laboratory have used a bridge bonding technique to combine an array of 32 x 32 APD with a timing circuitry chip<sup>11,12</sup>. After the two dies are bonded with epoxy, vias to interconnect the APDs to the readout are formed in the bridge bonding process. In terms of labor the bonding process is expensive and the size of the vias limits the fill factor of the APDs to 13%. The driving force behind the DigitalAPD concept is to reduce the size of the active quenching circuitry while maintaining, low jitter, afterpulsing and noise and high quantum efficiency.

The aim of this research is show how quenching circuitry can be reduced by replacing the current active quench circuit and resistive quenching with a few simple digital switches. This paper shows initial prototype development of a single DigitalAPD cell that can be used as a replacement quench module in an existing photon counting product and an initial proof of concept demonstrator to show operation of an array of devices. DigitalAPD imaging devices have the potential to compete with intensified and electron-multiplying CCD arrays giving a less expensive compact solution with superior throughput that does not require extensive cooling. APD array readout circuitry has the potential to allow complete random access to any sensor which is not the case in the CCD devices.

## 2. METHODOLOGY

### 2.1 Single DigitalAPD device concept

The DigitalAPD takes advantage of the parasitic capacitance of the APD in reverse bias. This capacitance is typically in the range of 10fF for a 10 micron diameter device to 0.16pF for a larger 40 micron device. Parallels can be drawn between the DigitalAPD and a dynamic RAM device where the memory cell is refreshed at a defined rate. The concept is shown in Fig 3. The anode of the DigitalAPD is negatively biased at around the typical breakdown voltage. Initially in the sequence of operation, the APD is precharged on a write cycle to a voltage above the breakdown potential. The voltage source is then disconnected from the DigitalAPD but the voltage remains stored by the parasitic capacitance of the DigitalAPD. The DigitalAPD APD maintains the overvoltage over time as shown in Fig 3 unless a photon is incident on the devices active area. Such an incident photon would cause an avalanche breakdown and the charge would leak away. The voltage is therefore readout as a '0' if a photon is incident or a '1' if no photons were detected.

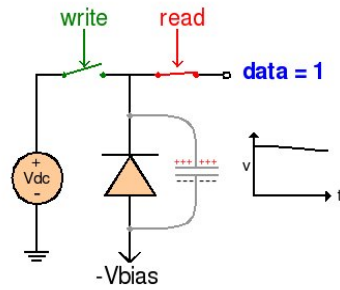


Figure 3: Concept of the DigitalAPD

## 2.2 DigitalAPD array imaging

An array of DigitalAPDs can be formed by arranging the single cells to be read out in a word format, each word forming a row of the array, as detailed in Fig. 4. Each cell contains a switch controlled by the word select input  $W_0$  to  $W_3$ . One side of the switch connects to the cathode of the APD and the other connects to a vertical bit line. For the  $4 \times 4$  array shown initially none of the word lines  $W_0$  to  $W_3$  are selected and the APDs have been charged to the voltage over breakdown. The APD bit lines are then connected to the buffer inputs. A word line can then be cyclically asserted in order to read the buffer output for a row of DigitalAPD cells. The bit lines can then be switched to the charge voltage then deselected before repeating the sequence for the next word. In comparison to the photon event driven approach generally used, a synchronous approach is taken here where the array can be scanned through and also any individual APDs or windows of interest can be sampled at a higher rates.

## 2.3 Charge sharing model

It is possible that the devices will be capable of directly driving logic from the voltage held on the capacitance of the junction. Therefore simply connecting the device cathode to a buffer or inverter may allow measurement of the device voltage (i.e. determine whether it has broken down or not). However, it is likely that the device may already be discharged a little and/or the capacitance of the device may be discharged as the gate and interconnect capacitance of the measuring buffer is charged. For this reason, in the first instance of the prototype, a charge transfer model will be assumed rather than a static voltage model. This means that we will assume that once the device is switched on to a node (i.e. a bit line) then charge will either flow off the device and onto the node (capacitance) or vice versa. Hence it can be assumed that the voltage of the node will either decrease or increase depending on the state of the APD. If we know the voltage of the node initially comparing this to the voltage of the node after the APD is switched in, allows us to determine if the node voltage has increased or decreased.

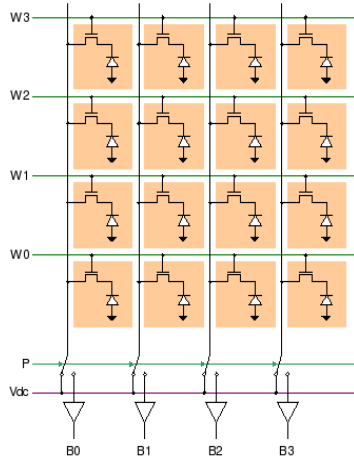


Figure 4: DigitalAPD array concept

The charge sharing between the APDs and the readout circuitry could potentially become an issue when the device switch is enabled. Consider that  $C_A$  is the capacitance on the APD side of the circuit and  $C_R$  is the capacitance at the readout side. If  $C_R$  is greater than  $C_A$  then charge sharing will be a problem. This is explained with referral to Fig 5. When the status of the APD data is '0' following an incident photon and the bit-line has been charged to a '1' by a previous read then when the word line is selected some charge flows onto the APD node. This increases the voltage of the cathode above the threshold that decides whether or the stored data is a '1' or a '0'. Conversely when the data stored is '1' and the bit line has been discharged to '0' by a previous read then charge flows from the APD node and could decrease the voltage to below the threshold. A crosstalk type effect could therefore be observed if  $C_A$  was less than  $C_R$ . Care must therefore be taken to select switches and buffers with very low capacitance and this will become more of an issue as the array size increases.

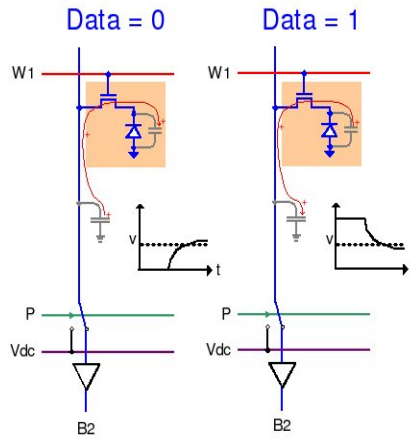


Figure 5: Charge sharing issues

## 2.4 Bit-line pre-charge solution

A solution to the charge sharing issue is to pre-charge the bit-lines to a known voltage before the read cycle. This voltage could be half way between the initial voltage on the APD cathode ( $V_{dc}$ ) and ground. This is similar to the principle of operation of DRAM. During the read cycle the bit line voltage will either increase or decrease depending on the occurrence of a photon event. The comparator is then used to detect the relative change in the bit-line voltage by comparing with  $V_{dc}/2$ . To implement the pre-charge a row of switches is used to select the charge voltage for the APD ( $V_{dc}$ ), the pre-charge voltage for the bit-line ( $V_{dc}/2$ ) or the buffer input (Fig 6).

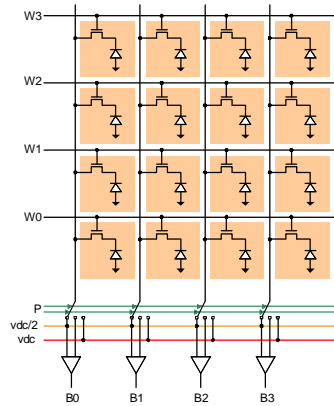


Figure 6: Bit-line pre-charge solution

## 2.5 Read and pre-charge process flows

The process to determine whether or not a device has broken down is as follows and outlined in Fig 7.:

1. Assert the P switch control lines such that the bit line is connected to  $V_{dd}/2$ . This ensures that the capacitance of the bit line is charged to around half the supply voltage before you connect the APD.
2. Assert the P control lines such that the bit line is now connected to the other comparator input, ready for the read.
3. Assert the word line so that the APD is now connected to the bit line. If the APD has broken down then the voltage across it will be lower than the bit line and so the bit line should drop down. If the APD has not broken down then the voltage across it should be around  $V_{dd}$  and hence the bit line should increase in voltage. Once the voltage of the bit line has settled, the output of the comparator should show whether the APD has broken down ('0') or not ('1').
4. The buffer output BO is written to memory
5. The APD parasitic capacitance is charged back up to  $V_{dd}$  by asserting the P control lines accordingly.
6. The word line is unasserted and the process moved onto the next word line.

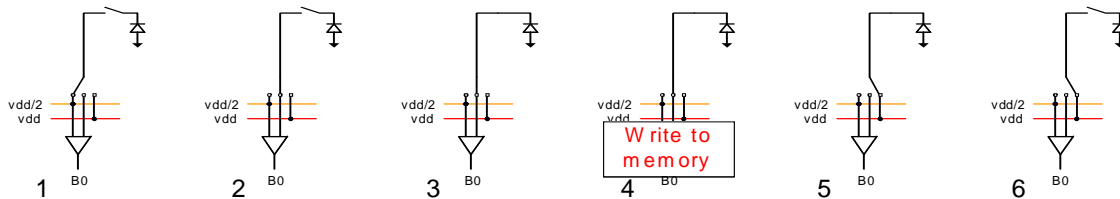


Figure 7: Bit-line pre-charge solution

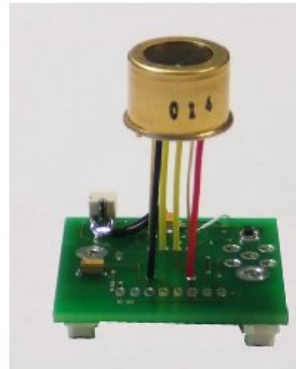
### 3. PROTOTYPE SYSTEMS

#### 3.1 PCDMini single cell DigitalAPD

SensL's Miniature Photon Counting devices are Geiger mode diodes with an incorporated quench circuit. SensL produce a photon counting platform called the PCDMini<sup>9</sup>. The PCDMini miniature photon counting device has a tiered structure with add-on modules available to enhance functionality (Fig. 8a). The basic device is a photon counting sensor with an active quench circuit on a small PCB board. This PCB is housed within a heat-sink that measures 35mm x 35mm in area. Stackable connectors provide an interconnection bus system so that add-on modules can be attached to the basic test board. The add-on modules include a peltier cooler driver circuit to enable the device to operate down to -20C. A PC interface module includes an integrated counter enabling the upload to and display of the count rate on a monitor using SensL integrated software tools. The platform is ideal for prototyping of new quench circuits. The communications add-on module has an SMA 50 ohm line driver output for direct connection of count pulses to an oscilloscope and a series of voltages can be supplied through the bus system. The communication module also contains a to d conversion so that voltages in the quench board can be monitored from the PC. A single cell DigitalAPD prototyping PCD was designed as a drop in replacement to the standard and allowed experimentation on the concept using a simple 2-layer FR4 PCB as shown in Fig 8b.



(a)



(b)

Figure 8: (a) SensL's PCDMini photon counting platform comprising of APD, heatsink, active quench module, peltier cooling module and communications module, (b) the digitalAPD alternative to the quench circuit.

#### 3.2 DigitalAPD array

For the prototyping of the DigitalAPD array it was decided to design a 4 by 4 APD version containing 16 APDs. This was big enough to demonstrate the array concept while still being manageable in size for any modifications that may be required during prototyping. Accurate timing of control signals for the array is crucial to the success of the DigitalAPD array and for this reason a FPGA (Field Programmable Gate Array) was included at the heart of the prototype (Fig 9). The FPGA controls the sequence required for the switches, effectively interfacing the APD via the output of the comparators to the memory. The controller was written in VHDL and downloaded to the FPGA. The circuit contains an on-board 2MB static memory device, to allow a burst of data to be stored in real-time via FPGA control. The FPGA also allows the memory contents to be read to a micro-controller device which was connected to the PC via a USB cable using the a propriety SensL protocol. The assembled PCBs are shown in Fig 10.

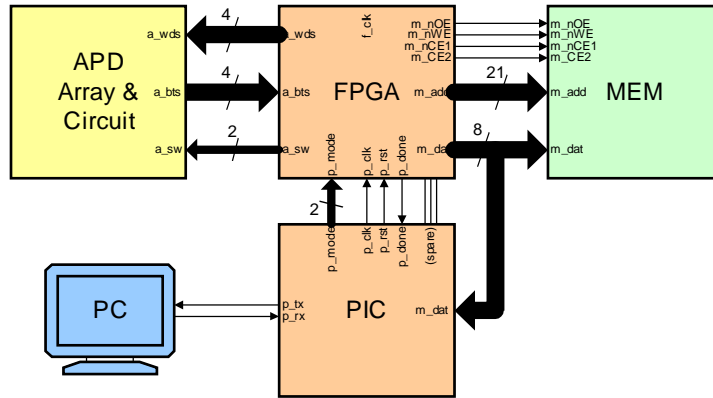


Figure 9: DigitalAPD array prototyping system

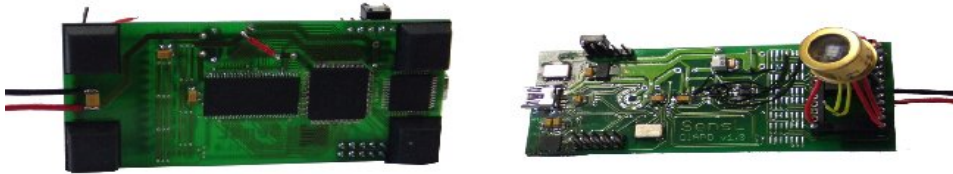


Figure 10: DigitalAPD array prototype PCB top and bottom views

## 4. RESULTS

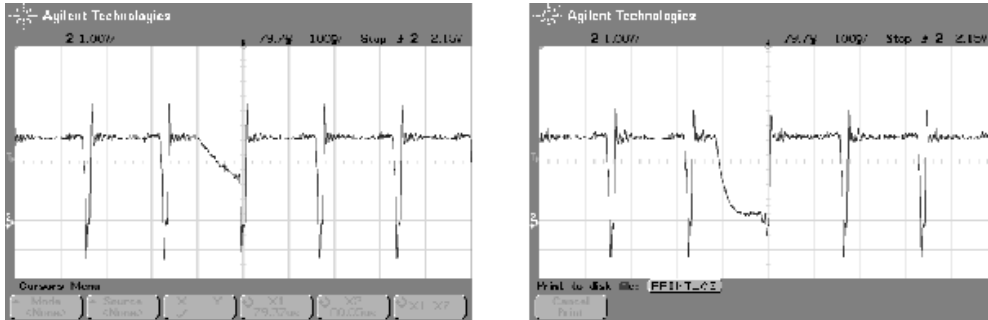
### 4.1 Charge sharing analysis in the DigitalAPD

The single cell and array prototyping platforms were successfully assembled to allow analysis and development of the DigitalAPD concept. As discussed in section 2 it was originally thought possible that the devices would be capable of directly driving logic from the voltage held on the capacitance of their junction. However, this was found not to be the case, since connecting the device anodes to anything alters the stored voltage. This is because the charge on the cathode has to 'charge' whatever it has just been connected to transfer its voltage, and this charge sharing significantly changes the voltage stored since the capacitance of the APD is so small. Furthermore, the voltage drops more slowly than was previously thought so the signals would be unlikely to cross a buffer threshold within the sample period. This proved to be more of a problem with the smaller area devices such as the 10 micron diameter APDs. Although these devices have less charge to disperse due to their lower capacity the avalanche effect is considerably less leading to a slower discharge. The threshold voltages for the comparator therefore had to be carefully set and the variable voltage reference on the single cell module was used to find the optimal setting.

To circumvent the charge sharing problem a pre-charging solution was originally proposed. However, this pre-charge step did not prove to be effective, presumably because the clock feed-through from the switch control line activity appears to be more considerable than originally thought. This effect could possibly be reduced in the future by looking for switches with a better isolation and more advanced multilayer PCB design using ground planes and digital signal isolation.

## 4.2 Additional quench circuitry

It was found to be very important to quench the APDs down to ground actively because after pulsing results if they don't quench themselves fast enough. Since the bit-line pre-charge phase was proving problematic this phase was replaced by the quench. The quenching is only across a potential difference of 5V and so this can be achieved fairly easily using standard logic. Fig. 11 shows the waveforms observed at the cathode of (a) 10 micron and (b) 40 micron diameter DigitalAPD. Each of the traces show a series of samples and one photon being detected in each trace. This is denoted by the early self quenching at approximately 50ns after the quench pulse. The current prototype of the DigitalAPD runs at over 5MHz sampling rate



(a)

(b)

Figure 11: Waveforms observed at the cathode of (a) 10 micron and (b) 40 micron devices.

## 4.3 Jitter and time walk analysis

Jitter and time-walk of the single digital APD cell were measured using a Becker & Hickel SPC-140 counting PCI card<sup>14</sup> and the results are shown in Fig. 12. The results proved favorable for such a basic PCB design. The FWHM jitter recorded was in the order of 162ps at 50kcps and 169ps at 500kcps. Time walk between these plots was approximately 50ps. It is estimated that these results could be improved considerably by optimising the PCB design.

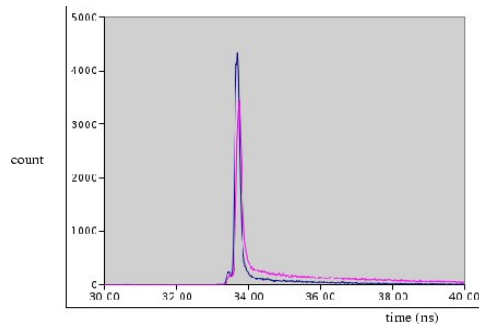


Figure 12: Jitter and time walk analysis at 50kcps and 500kcps

## 5. CONCLUSIONS

This paper has proposed a new concept for Photon counting applications, the DigitalAPD. The concept makes use of the parasitic capacitance of the APD to store a charge. Photons striking the APD active area cause the charge to be lost in the avalanche breakdown and detection of the voltage across the APD after a set time interval can be used to determine whether or a photon event has occurred.

The concept has been demonstrated on a single DigitalAPD module compatible with the PCMini photon counting system and an architecture for a DigitalAPD for use in low light level imaging applications has been proposed and also demonstrated. The architecture draws some parallels with that of DRAM in that the cells must be cyclically recharged before reading. A 4 by 4 array has been prototyped and results have been taken at word line rates of up to 5MHz. It is estimated that with optimisation then cycle periods down to 10ns may be achieved. The simplicity of the DigitalAPD in terms of the number of components per cell and manageable voltages involved make this type of device very attractive for implementation in larger arrays.

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