Fully integrated sub 100ps photon counting platform

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ABSTRACT

Current state of the art high resolution counting modules, specifically designed for high timing resolution applications, are largely based on a computer card format. This has tended to result in a costly solution that is restricted to the computer it resides in. We describe a four channel timing module that interfaces to a computer via a USB port and operates with a resolution of less than 100 picoseconds. The core design of the system is an advanced field programmable gate array (FPGA) interfacing to a precision time interval measurement module, mass memory block and a high speed USB 2.0 serial data port. The FPGA design allows the module to operate in a number of modes allowing both continuous recording of photon events (time-tagging) and repetitive time binning. In time-tag mode the system reports, for each photon event, the high resolution time along with the chronological time (macro time) and the channel ID. The time-tags are uploaded in real time to a host computer via a high speed USB port allowing continuous storage to computer memory of up to 4 millions photons per second. In time-bin mode, binning is carried out with count rates up to 10 million photons per second. Each curve resides in a block of 128,000 time-bins each with a resolution programmable down to less than 100 picoseconds. Each bin has a limit of 65535 hits allowing autonomous curve recording until a bin reaches the maximum count or the system is commanded to halt. Due to the large memory storage, several curves/experiments can be stored in the system prior to uploading to the host computer for analysis. This makes this module ideal for integration into high timing resolution specific applications such as laser ranging and fluorescence lifetime imaging using techniques such as time correlated single photon counting (TCSPC).

Keywords: Geiger Mode avalanche photodiodes, Photon Counting, APD, TCSPC, time-tagging, FPGA.

1.INTRODUCTION

The use of low light detection[1] is a requirement in many existing and emerging fields such as the life sciences, biomedical engineering, cell imaging, bio-analytical equipment[3], nuclear medicine, radiation detection, high energy physics, and laser ranging and 3D imaging. In particular low light detection combined with high resolution timing has enabled the life sciences, through techniques such as fluorescence lifetime imaging (FLIM) which have been used from DNA to protein to fingerprint detection[4,5,6]. Techniques such as time correlated single photon counting[7] and fluorescence resonance energy transfer (FRET)[8] illustrate the power of timing photons of light using high resolution timing equipment. In high time resolution range finding, using pulsed techniques it is possible to measure directly the return time of individual photons. Since photons travel at the speed of light (3E8meters/second), it is important that high resolution timing hardware is available to determine accurately small distance[9,10]. In many of these applications the requirements are to time the arrival time of the photon down to levels which are sub picosecond, This allows the measurement of sub nanosecond lifetimes in FLIM and high resolution timing resolution down to sub centimeters in laser ranging. The basis for a system which a
llows sub 100 picosecond timing resolution will be shown in the subsequent sections.

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2.HRMTime SYSTEM DESCRIPTION

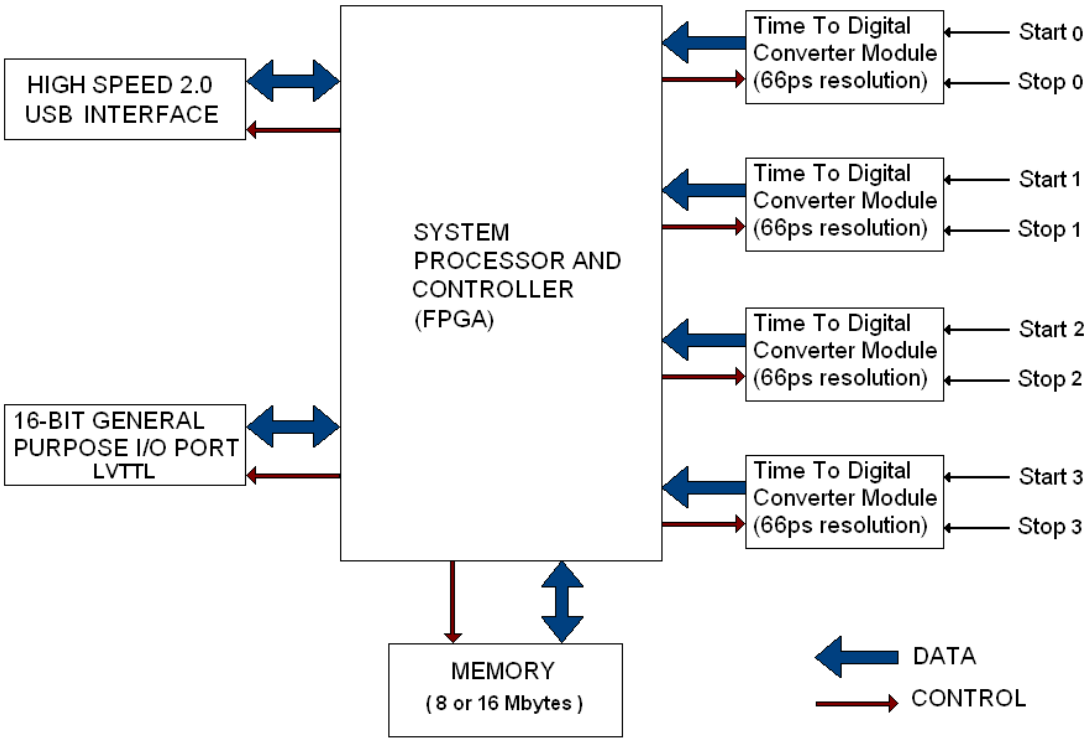


Fig 1. HRMTime Block Diagram

The HRMTime system consists of 4 'time to digital' modules, 16 I/O ports, a high speed USB interface, memory storage and an FPGA based processor. The purpose of each element is as follows.

2.1 Memory

The memory module is a HRMTime format plug-in mezzanine board providing 8, or 16 Mbytes of memory.

2.2 Time To Digital Converter Module

This module is the front end of the system and is responsible for resolving the timing between the start and stop inputs of each of up to four channels. Each channel is controlled by the FPGA and can be programmed to start and stop on either LO-HI or HI-LO transitions.

2.3 High Speed USB 2.0 Interface

The USB interface is used to command/configure the HRMTime as well as download, in real-time, time-tag data to the host computer. This USB interface implements high speed USB 2.0 protocol allowing real time continuous logging of time-tag data up to rates of 5MHz without data loss.

2.4 16-bit General Purpose I/O Port

This general purpose I/O port is used to allow multi-dimensional curve readings. The position of curve data, within the system memory, can be defined by these ports. These ports can be set directly by outside control lines (inputs) or by software to drive outside equipments (outputs).

2.5 System Processor and Controller

The 'System Processor / Controller' is implemented in a 464 pin BGA FPGA and is responsible for implementing all the functionality of the HRMTime module. This section decodes commands from the USB and executes the time-bin or time-tag function accordingly. All results are saved in memory as time-bins for curve measurements or time-tags for continuous recording. In this latter mode the memory is configured as a large FIFO to allow continuous downloading of time-tag data up to rages of 5MHz.

3.HRMTime TYPICAL APPLICATION

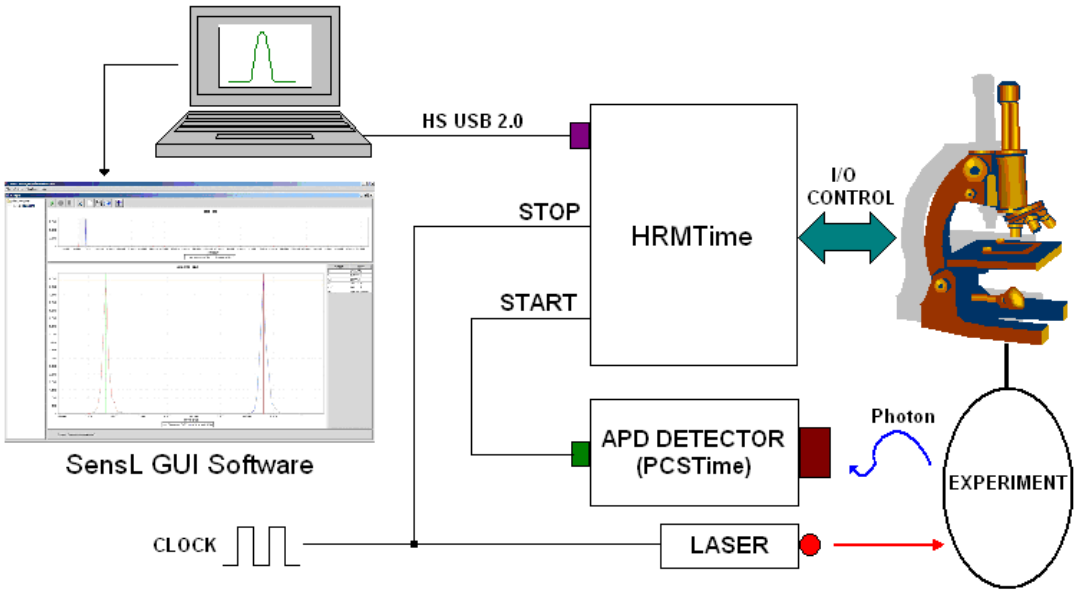


Fig. 2. Typical Application Block Diagram

Fig 2 shows a typical application setup utilizing a wide range of the HRMTime features. In this example the experiment is a TCSPC application where a LASER is stimulated by a clock and the time before a photon is detected is measured.

The LASER is continually pulsed at a fixed frequency (typically 50MHz). The LASER output will affect a setup resulting in a photon arriving at the APD Detector such as the SensL PCSTime[11], PCMPlus[11] or PCDMini[12]. It is assumed that the rate of photons arriving at the APD is far less than the rate of the LASER pulses. As a photon is not guaranteed for each cycle of the LASER, the system will use the photon event as the start of the TCSPC[13] process and a delayed version of the LASER pulse as the stop signal. This technique avoids countless dead cycles and simplifies the associated electronics required for recording the events.

The HRMTime module measures and records the time delay between clock and photon from the experiment and uploads the results, in real time, to the host computer via the USB interface. In some cases the experiment will involve multiple TCSPC curve measurements as the experiment changes the settings of external equipment. The programmable I/O of the HRMTime module is used to cater for such applications. The external equipment, such as a microscope, can indicate its X,Y movement to the HRMTime module allowing multiple curves to be measured. Alternatively, the HRMTime module can be programmed as outputs to control the external equipment and cause the actual X,Y positioning of the equipment.

4.SYSTEM PROCESSOR AND CONTROLLER DETAILED DESCRIPTION

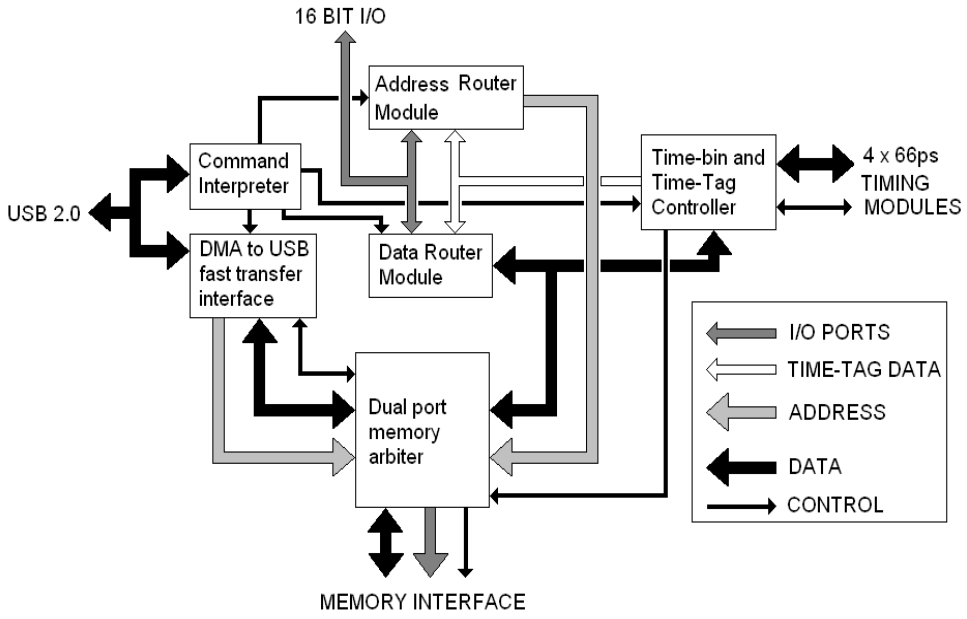


Fig. 3. System Processor and Controller Block Diagram

The 'System Processor / Controller' is implemented in a 464 pin BGA FPGA. Fig 3 shows a simplified block diagram of the design within this device.

4.1 Command Interpreter

This module is responsible for receiving a set of commands from the host computer and controlling the system accordingly. HRMTime is a fully programmable system with a wide range of parameters that can be user defined. The **Command Interpreter** is responsible for setting these parameters and starting the execution of a particular task.

4.2 DMA to USB Fast Transfer Interface

The system memory is dual ported between the USB and the Time-Bin / Time-Tag controller. This module controls the reading of data from memory to the USB interface by means of high speed DMA block transfers. The **Command Interpreter** initializes this module with a start address and block data count. When commanded to start, this module interfaces with the **Dual Port Memory Arbiter** to read the pre-programmed data block. The rate of this process is such that data can be transferred from the memory to the USB port as fast as required. This allows the USB 2.0 high speed interface to operate at full speed without loss of data.

4.3 Time-Bin and Time-Tag Controller

This module is responsible for carrying out the particular Time-Tag or Time-Bin process as defined by the **Command Interpreter**. This module communicates with the **Timing Modules** and saves the results of the measurements in the dual ported memory. The format of these results is determined by the mode of operation. In time-bin mode, this module will use the time information from the **Timing Modules** to determine the particular bin to be incremented. In time-tag mode this module will treat the memory as a large FIFO, saving time-tag data in consecutive locations. The format of the time-tag data is determined by the **Data Router Module**.

4.4 Data Router Module

The **Data Router Module** is a complex programmable multiplexer that allows any, of a wide range of inputs, to be routed to any of the 32 memory data bits. In time-bin mode this module is bypassed to allow the **Time-Bin and Time-Tag Controller** to directly access the memory for the purpose of incrementing time-bins. In Time-Tag mode this module determines the format of the time-tag data. The **Command Interpreter** presets the routing of this module to

define which bits of the time-tag are Time-Tag data (both Micro and Macro) from the **Time-Bin and Time-Tag Controller** and I/O data from external equipments.

4.5 Address Router Module

The **Address Router Module** is a complex programmable multiplexer that allows any, of a wide range of inputs plus an internal address counter, to be routed to any of the memory address lines. In time-tag mode this module will normally be programmed to present the internal address counter bits as the memory address. The internal address counter automatically increments after each memory write creating a FIFO type interface. In time-bin mode the **Command Interpreter** presets the routing of this module to a mix of the address counter, time-tag data and I/O data. Routing the time-tag data to the address will create a range of consecutive bins separated by the time resolution of the LSB. The address counter bits can be used to define the base address of a particular curve whilst the I/O data can be used by external equipments to move the curve for multi-dimensional measurements.

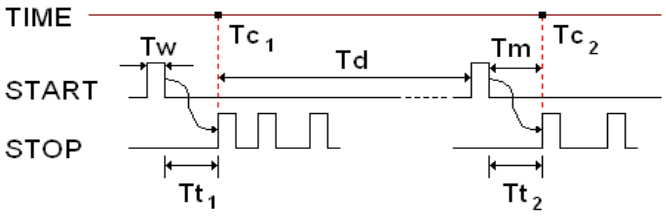
4.6 Dual Port Memory Arbiter

This module controls the data transfers to/from system memory to the USB and Time-Bin / Time-Tag Controller. Each port presents an address, direction (R/W) and request signal. This module detects the particular request, carries out the memory access and directs the data to/from the requesting port at the requested address.

5.HRMTime MODES OF OPERATION

Whilst the HRMTime module is designed as a generic high resolution time measurement instrument, it is envisaged that it will be most used in photon counting experiments. For this reason the modes of operation for the module have been designed with this in mind.

5.1 Time-Tagging with TCSPC



Tt = MICRO Time (TPSPC time)
Tc = MACRO Time (Chronological Time)

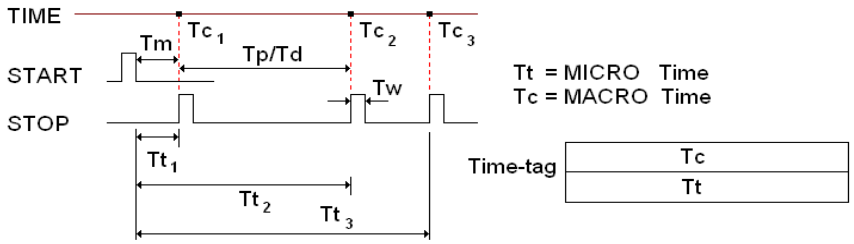
Time-tag	Tc	Tt

Tw	Minimum Start or Stop input pulse width	1.5ns
Td	Minimum time to process event (dead time)	190ns
Tt	TCSPC resolution (LSB)	30ps
Tm	Minimim time from Start to Stop	5.2ns
Tc	Chronological time resolution (LSB)	5ns

Fig. 4. Time-Tagging with TCSPC

In this mode the start of each channel will be the photon event and the stop will be a delayed version of the laser clock. On receipt of an event the time-tag will be read and the 66ps timing module will be immediately reset. The reset will clear the channel ready for the next photon event. All subsequent stop pulses will be ignored until a new start pulse arrives. Each time-stamp will be a 32-bit word describing the TCSPC time (micro-time Tt) and the value of a free running clock defining the time within the experiment (macro-time Tc). Due to the highly flexible **Data Routing Module** the resolution and number of bits for the micro time, macro time and channel ID bits is selectable using the USB selection registers. When this process begins, 32-bit time-tags will be inserted into the shared memory. The memory will be configured as a large FIFO interfacing to the USB interface. Suitable handshake signals are implemented allowing continuous transfer of time-tags from the FIFO to the PC via the USB port. With counts of up to 5MHz this process can run indefinitely without loss of data.

5.2 Continuous Time-Tagging



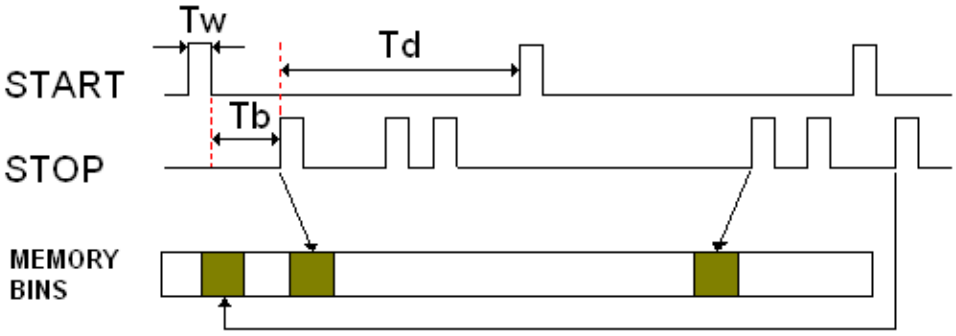
Tw	Minimum Start or Stop input pulse width	1.5ns
Tp	Minimum time between Stops (Note 1)	5.5ns
Td	Maximum average Stop rate (Note 1)	190ns
Tt	Time-Tag resolution (LSB)	30ps
Tm	Minimim time from Start to first Stop	5.2ns
Tc	Chronological time resolution (LSB)	5ns

Note 1: The time to process an event (dead time) is the same as for TCSPC (190ns). However, the time measurment modules have a 256 deep FIFO allowing bursts in excess of 150MHz.

Fig. 5. Continuous Time-Tagging

In this mode a single start pulse will be applied to all channels. After this event all photons will be time-stamped and saved the the memory. As this will be continuous the time-tag is extended to allow very long periods of recoding without wrap-round. Each time-tag will comprise of two 32-bit words. The first word will provide the time-stamp to a resolution of 66ps. This high resolution timing value will wrap-round after 5us. On each wrap-round an 8-bit counter will be incremented. This counter will also reside in the first 32-bit word with the channel ID bits. The MSB of the 8-bit counter is used to increment a 32-bit counter. This counter will be stored as the second 32-bit word of the time-tag. Hence the 8-bit counter and the 32-bit second word form a 40-bit wrap-round counter where the LSB is 5us. The memory will be configured as a large FIFO interfacing to the USB interface. Suitable handshake signals are implemented allowing continuous transfer of these time-tags from the FIFO to the PC via the USB port.

5.3 Time-Binning with TCSPC

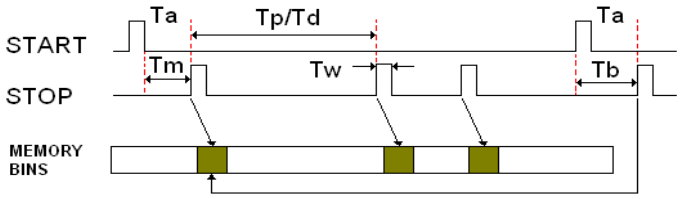


Tw	Minimum Start or Stop input pulse width	1.5ns
Td	Minimum time to process event (dead time)	190ns
Tb	Minimum BIN size	30ps

Fig. 6. Time-Binning with TCSPC

In this mode the start of each channel will be the photon event and the stop will be a delayed version of the laser clock. On receipt of an event the time-tag will be read and then the timing module will immediately be reset. The reset will clear the channel ready for the next photon event. Each time-stamp from the timing module will be used as an address to increment a memory location (Time-Bin). The resolution of the bins and the position of the curve in memory will be defined by the highly flexible **Address Routing Module**. As previously explained, the time-tag, address counter and I/O bits can all be routed to the memory address lines. This flexibility allows many TCSPC options from a simple single curve to multiple curved defined by the address counter and external control from the I/O port.

5.4 Continuous Time-Binning



Tw	Minimum Start or Stop input pulse width	1.5ns
Tp	Minimum time between Stops (Note 1)	5.5ns
Td	Maximum average Stop rate (Note 1)	190ns
Tb	Minimum BIN size	30ps
Tm	Minimim time from Start to first Stop	5.2ns

Note 1: The time to process an event (dead time) is the same as for TCSPC (190ns). However, the time measurment modules have a 256 deep FIFO allowing bursts in excess of 150MHz.

Fig. 7. Continuous Time-Binning

In this mode the start signal is a low frequency clock (less than 7 MHz). The stop signals will be the photon events. Unlike the TCSPC mode, the 66ps timing module is not reset after the first photon event. Due to the long clock period it will be possible for the same channel to receive a number of photons per clock cycle. Hence, in this mode the time-bins will fill up to plot the occurrence of photons over the period of the clock cycle. Each new start signal will reset the 66ps timing module. This allows the system to build up a plot of all the photon events within the start pulse cycle. Once again the flexibility of the **Address Routing Register** provides a wide range of options from single to multiple curves. In the example shown in Fig 7, the first photon after each start occurs at the same time bin. Hence this bin will be incremented twice.

6.RESULTS AND DESIGN VALIDATION

To validate the accuracy of the HRMTime module it was necessary to compare the results with established commercially available equipment.

Equipment used:

Becker & Hickl SPC-140[14]	PCI timer card with resolution of 6ps
HP8131A[15]	Resolution of 58ps

6.1 Jitter

To determine the jitter of the HRMTime module the HP8131A was setup to generate a square waveform with a period of 1us. The high pulse was varied from 50ns to 55ns in 10ps steps. The standard output was used as the start and the compliment output used as the stop. Hence the timer module (SPC-140 or HRMTime) will measure the duration of the high pulse.

First the SPC-140 was used to measure the jitter. This value was measured to be 58ps (FWHM) and appeared to be consistent from 50 to 55ns.

The HRMTime was then run in TCSPC mode using the same waveforms. For each time between 50 and 55ns the bins were saved and plotted. It was found that all measurements occurred in 7 to 8 consecutive 30ps bins. It was found that the shape of the plot of these bins varied as the time moved across the boundary of the 30ps bin resolution.

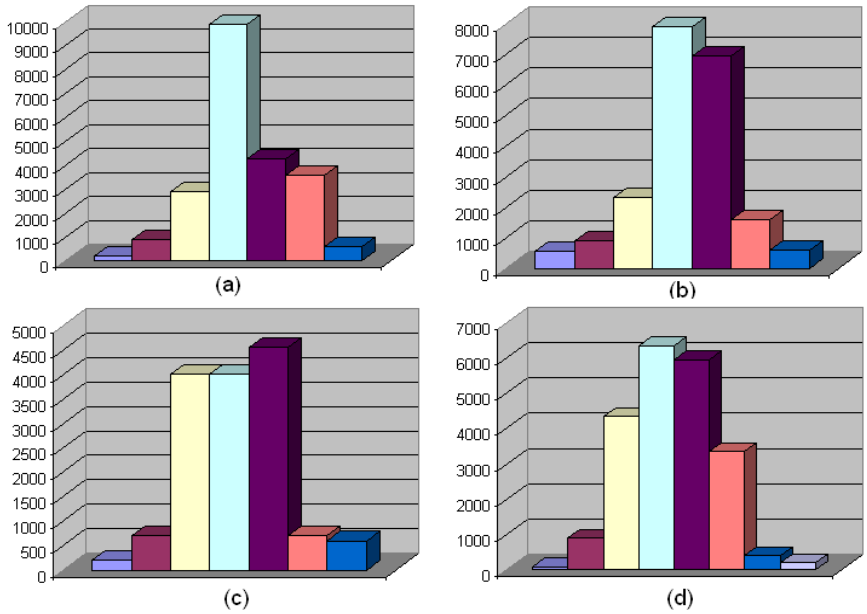


Fig. 8. Typical Bin Distribution Measurements

A typical example of this is shown in figure 8. Here four consecutive measurements (10ps apart) are plotted as histograms. It can be seen that the effective FWHM of the reading varies considerably as the time to measure changes from central of a bin (a) to the boundary of 2 consecutive bins (c and d).

To determine if the inherent jitter of the HRMTime was acceptable the jitter of the HP8131A had to be removed from the experiment. Now the jitter of the system is the square root of the sum of jitter of the source squared (HP8131A) and the detector squared (SPC-140 or HRMTime).

Therefore:

$$J(t) = \sqrt{J(s)^2 + J(d)^2}$$

J(t) = Total system jitter
J(s) = Jitter of source
j(d) = Jitter of detector

For the SPC-140:

J(t) = 58ps and J(s) = 6ps.

Therefore, using the above formula, the jitter due to J(s) is ~ **58ps**

Note: The jitter of the SPC-140 is negligible compared to the HP8131A.

For the HRMTime:

J(d) = 66ps and J(s) = 58ps

Note: The timing module used by HRMTime was designed with a 66ps (FWHM) resolution.

Therefore, using the above formula, the total expected system jitter J(t) ~ **88ps.**

This value of 88ps corresponds to 3 bins which agree most favorably with the experimental results shown in figure 8.

6.2 Timing Measurement

To determine the accuracy of the HRMTime time measurements the HP8131A was setup to generate a square waveform with a period of 1us. The high pulse was set to 50ns.

The output of the HP8131A was fed directly to the start input of the detector (SPC-140 or HRMTime) and also to the input of a test box. Details of this test box are shown in figure 9.

The output of the test box is connected via an SMA cable to the stop input of the detector. This SMA cable, at the output of the test box, is made long to ensure that the stop occurs after the start pulse. The switch, when in position (a), feeds the input directly to the output. When the switch is in position (b) the input is fed to the output via the test cable. Hence the delay through the box will vary depending on switch position and the length of the test cable.

With a test cable connected and the switch in position (a) a TCSPC curve was measured and saved. The switch was then put into position (b) and a second TCSPC curve was measured.

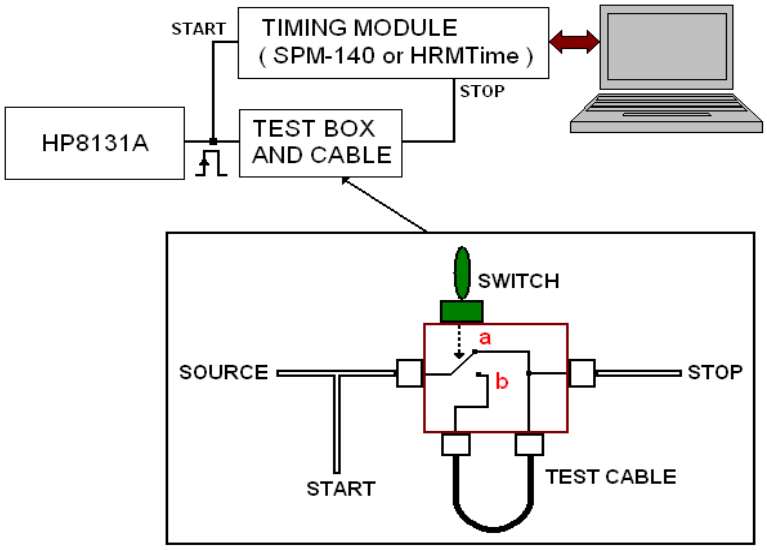


Fig. 9. Measurement Test Setup

The time difference between each TCSPC curve was then measured. The time difference between the peaks is the result of the delay due to the TEST CABLE and associated connections. This experiment was carried out for a number of different length cables and the delay for HRMtime and the SPC-140 compared. Fig 10 and Fig 11 show typical results for a given cable.

The time difference between peaks as measured using the SPC-140 (Fig 10) is 1.467ns.
The time difference between peaks as measured using the HRMTime and the SensL Integrated Environment GUI is 1.482ns.

The difference between the two measurements is 15ps (half a bin period of the HRMTime).

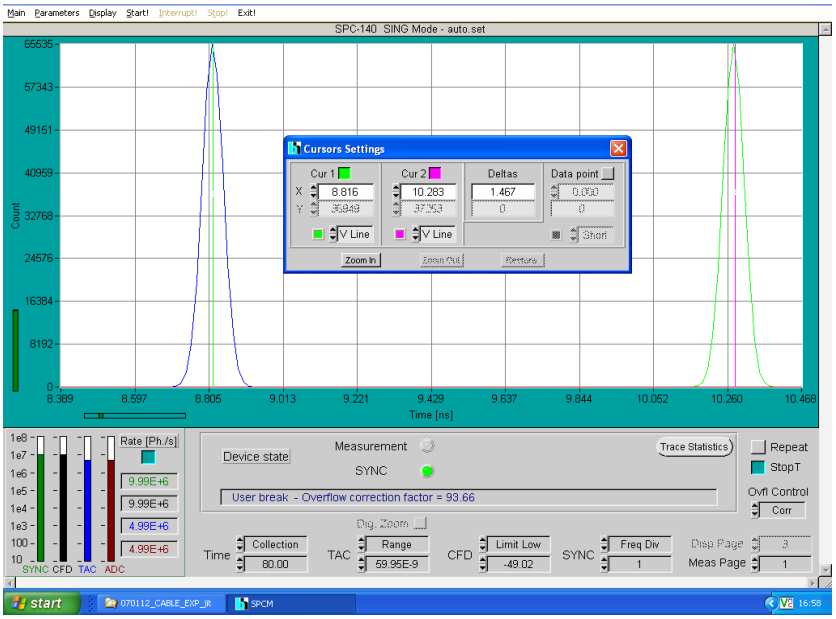


Fig. 10. Becker and Hickl SPM-140 Measurement

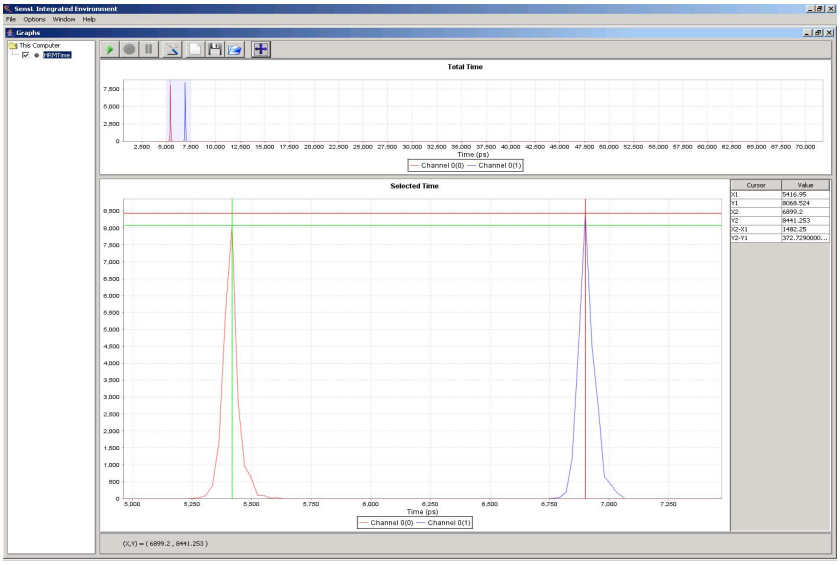


Fig. 11. SensL Integrated Environment Measurement

7.CONCLUSIONS

Previous high resolution, multi-channel, counting modules, specifically designed for TCSPC applications, have tended to be based on a computer card format such as PCI. This has tended to result in a costly solution that is restricted to the computer it resides in.

The HRMTime module has shown that multi-channel high resolution timing modules can be developed that can interface to a host PC without the restrictions imposed by the PCI data bus. The HRMTime has been shown to successfully interface to a PC (including LAPTOP) using high speed USB 2.0 and continuously record TCSPC data at rates of 5MHz without loss of data.

The HRMTime module was tested and shown to perform with a timing resolution of 66ps and, using long TCSPC runs of many readings resolve time durations down to the single minimum bin size of 30ps.

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