

# Progress in Quenching Circuits for Single Photon Avalanche Diodes

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**Abstract**—An ever wider variety of applications employ Single Photon Avalanche Diodes (SPADs) for the detection of faint optical signals. SPADs are p-n junction biased above the breakdown voltage and operate in Geiger-mode: each electron-hole pair can trigger an avalanche multiplication process that causes the current to swiftly rise to its final value. Additional quenching electronics is necessary for a SPAD proper working. The additional electronics characteristics directly affect the system's obtainable performances. Different quenching circuits affect the detector performances in different ways. In the last 15 years there has been considerable development in the integration of the quenching circuitry directly with the detector, thus leading to improved performances. This paper reviews the state of the art of this evolution, examining and comparing different classes of quenching circuits and explaining their mode of operations, their advantages and disadvantages.

**Index Terms**—Avalanche photodiodes, quenching circuits, single-photon avalanche diode (SPAD).

## I. INTRODUCTION

ANY applications nowadays employ, for the detection of very faint optical signals, avalanche photodiodes instead of photomultipliers, due to the advantages of solid state detectors (miniature size, lower voltage operation, higher quantum efficiency, insensitiveness to magnetic fields). The traditional Avalanche PhotoDiode (APD) is biased at a voltage near, but below, breakdown, and takes advantage of the avalanche multiplication process to obtain a measurable current signal by amplifying the photogenerated current. However, the statistical fluctuations in the multiplication process are amplified as well, thus limiting the maximum achievable gain. Another kind of avalanche detector is obtaining an ever more widespread diffusion: the Single Photon Avalanche Diode (SPAD). SPADs differ from APDs in being biased above breakdown, so exploiting the avalanche multiplication process in a different way: when an electron-hole pair is generated

(either thermally or by photon absorption) the carriers are accelerated by the high electric field until they impact ionize, thus generating additional carrier pairs; these pairs are in turn accelerated until ionization. A positive feedback loop is established, causing the current to swiftly rise to its final value, limited only by the excess bias above breakdown voltage and the series resistance due to space charge effects. Therefore, SPADs do not linearly amplify the current like APDs, but operate in the so-called Geiger Mode: an avalanche current reaches a standard final value whether it has been triggered by only one or many carrier pairs.

However, Geiger mode operation means that, once triggered, the avalanche final current keeps on flowing, thus rendering the device useless for subsequent detections. The avalanche process must therefore be stopped and later the device must be brought back into its original quiescent state: that is the duty of the quenching circuits.

The interruption of the avalanche multiplication process is called “quenching.” The time elapsed from onset until the avalanche is quenched is called “quenching time.” The later procedure is called “reset,” and the “reset time” is the time taken to bring the device back to its original state.

Quenching circuits' features directly affect the performances obtainable by the device. For example, a slow quenching circuit will limit the maximum counting rate, or it may impair the timing response. It is therefore important to choose the quenching circuit most suitable to the desired application. In the last 15 years, quenching circuits have been further developed to improve the total system performances.

In this article we will examine different classes of quenching circuits, for each explaining the mode of operation and detailing their advantages and disadvantages, focussing on performance improvement due to direct integration with the detector.

## II. PASSIVE QUENCHING CIRCUITS

As stated in the previous section, once an avalanche has been triggered, the avalanche current must be quenched. This can be achieved by lowering the SPAD's bias voltage below breakdown, preventing the multiplication process from taking place. The simplest way to accomplish this is by using a Passive Quenching Circuit (PQC), that consists of an high-value ballast resistor  $R_B$  connected in series to the diode (see Fig. 1).

In quiescent conditions, the SPAD is biased to the desired voltage through the ballast resistor. When an avalanche is triggered, the current swiftly rises to its peak value, given by the excess bias voltage  $V_{EX}$  divided by the SPAD's series resistance  $R_S$ . This current discharges the parasitic capacitance  $C_P$  at the

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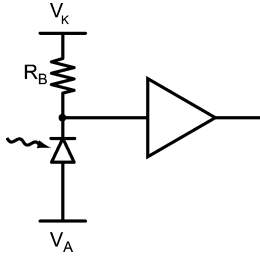


Fig. 1. Basic schematic diagram of a PQC.

SPAD cathode, so the excess voltage decreases exponentially towards zero with a time constant given by

$$\tau = C_P(R_S \parallel R_B). \quad (1)$$

The overall bias voltage, however, never descends below the breakdown voltage, so the avalanche is not, in fact, quenched, and current continues to flow through the device. The current final value is approximately the excess bias voltage divided by the ballast resistance:

$$I_F \simeq \frac{V_{EX}}{R_B}. \quad (2)$$

If this final value is high enough, the avalanche is self-sustaining, since enough carriers are present at any one time in the space charge region. On the other hand, if  $I_F$  is small enough, there will be a high probability that, after a random time, all the carriers have left the space charge region, so avalanche multiplication can no longer take place and the avalanche will self-quench. The boundary between “high enough” and “low enough” is not sharply defined, although a value of about  $100 \mu\text{A}$  has often been used. This imposes a minimum value on the ballast resistor, that must be large enough to yield a low current. The avalanche process is statistical, however, so the quenching time is statistical as well.

In order to give a first order estimation, useful for comparisons among different circuits, the quenching time can be considered to be the instant the exponentially-decaying current crosses the “quenching threshold” (the  $100 \mu\text{A}$  mentioned earlier). Thus, the quenching time can be calculated as

$$t_Q = \tau \ln \left( \frac{I_0 - I_F}{I_S - I_F} \right) \quad (3)$$

where  $I_0 = V_{EX}/R_S$  is the peak initial value of the avalanche current, and  $I_S$  the quenching threshold.

For traditional circuits, with SPADs connected to an external ballast resistor, the parasitic capacitance  $C_P$  is large, even  $10 \text{ pF}$  as reported in [1] and [2]. With such a large capacitance, the quenching time constant and the total passive quenching time are large as well. Using  $R_B = 100 \text{ k}\Omega$ ,  $V_{EX} = 5 \text{ V}$  and

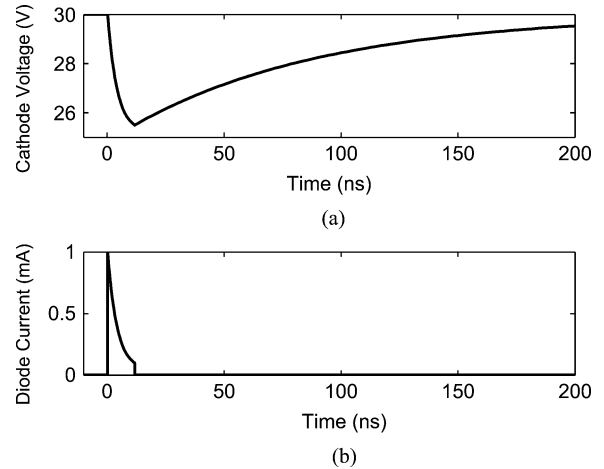


Fig. 2. (a) Cathode voltage and (b) Diode current waveforms for a SPAD connected to a PQC.

$R_S = 5 \text{ k}\Omega$ , the quenching time amounts to  $147 \text{ ns}$ . On the other hand, for more recent circuits with SPADs directly integrated with a PQC,  $C_P$  is much smaller, even less than  $1 \text{ pF}$ . Fig. 2 shows the cathode voltage and diode current waveforms for a SPAD with  $C_P = 1 \text{ pF}$  and the other parameters as above. As can be seen in the figure, the diode current starts from its peak value  $I_0 = 1 \text{ mA}$  and then decreases exponentially towards  $I_F = 50 \mu\text{A}$ ; meanwhile the cathode voltage also decreases exponentially. When the avalanche is quenched the current becomes zero, and the voltage slowly returns to its previous value. The passive quenching time in this case is about  $14.7 \text{ ns}$ , much smaller than the external case. Thanks to integration, the parasitic capacitance  $C_P$  can be even smaller, even down to  $70 \text{ fF}$  as reported in [3] for a  $7 \mu\text{m}$ —diameter SPAD. The smallest achievable parasitic capacitance is given by the intrinsic junction capacitance of the detector itself: assuming a  $1 \mu\text{m}$ —thick depleted region, for a reasonably sized  $50 \mu\text{m}$ —diameter SPAD, the junction capacitance is in the order of  $200 \text{ fF}$ . For this figure, keep in mind that the capacitance is proportional to the square of the diameter.

As will be explained in more detail later in this section, an important parameter for quenching circuits is the overall avalanche charge. The avalanche charge is given by the integral of the current flowing through the device from avalanche onset until quenching, and depends on the parasitic capacitance, the excess bias voltage and the quenching time. For a given excess bias voltage, the avalanche charge can be reduced in two ways: by decreasing the time taken to quench the avalanche, or by reducing the parasitic capacitance. A decrease in quenching time can be obtained by increasing the value of the ballast resistor: the current continues to decrease exponentially with almost the same time constant, but if the final value is smaller, the threshold  $I_S$  will be crossed earlier.

An example of different quenching times with different ballast resistors for a detector directly integrated with the quenching circuit is shown in Fig. 3; when  $R_B = 100 \text{ k}\Omega$  we

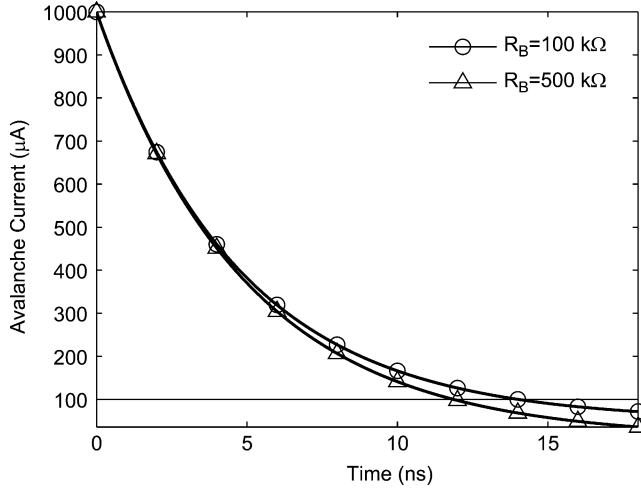


Fig. 3. Diode current waveform for different  $R_B$  values.

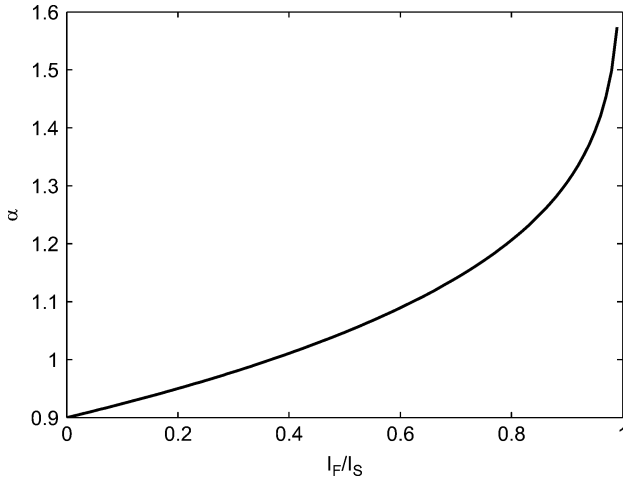


Fig. 4. Dependency of  $\alpha$  on  $I_F$ .

have  $I_F = 50 \mu\text{A}$  and  $t_Q = 14.7 \text{ ns}$ , whereas for  $R_B = 500 \text{ k}\Omega$ ,  $I_F = 10 \mu\text{A}$  and  $t_Q = 11.9 \text{ ns}$ .

Having defined the quenching time as the instant when the decreasing avalanche current crosses the  $100 \mu\text{A}$  threshold, the overall avalanche charge can be calculated as:

$$Q = V_{\text{EX}} C_P \left[ 1 + \frac{I_F \ln \left( \frac{I_0 - I_F}{I_S - I_F} \right) - I_S}{I_0} \right] = V_{\text{EX}} C_P \alpha \quad (4)$$

where  $V_{\text{EX}} C_P$  is the theoretical avalanche charge with infinite ballast resistance, and  $\alpha$  is a factor depending on  $I_F$ , once the diode and the excess bias voltage are chosen. For an external PQC, with the values given above, the total charge amounts to  $52.4 \text{ pC}$ . Compare this value to that obtained using an integrated PQC: the overall avalanche charge is about  $5.24 \text{ pC}$ .

The dependency of  $\alpha$  on  $I_F$  is shown in Fig. 4. As can be seen, for small values of  $I_F$  the avalanche charge will be small, since the avalanche will be quenched early on. However, if the final current is large, close to  $I_S$ , the avalanche charge will be larger than the theoretical value.

Furthermore, the avalanche charge is directly proportional to the parasitic capacitance, so every capacitance reduction leads to a charge reduction; this makes the advantages clear in integrating a PQC directly with the detector. Integration has the additional advantage of allowing easy fabrication of detector arrays with passive quenching, for example that reported in [3], since the resistor takes up a small silicon area compared to the detector itself. Moreover, SPADs fabricated in planar technology are not symmetrical: one terminal presents higher parasitic capacitance than the other, due to how the detector has been designed. It is therefore convenient to connect the ballast resistor to the less capacitive of the two terminals. Both options have been reported in literature, for example in [4], [5] the ballast resistor is connected to the diode's anode, whereas in [6], [7] the resistor is connected to the cathode.

But why is the avalanche charge such an important parameter? The energy dissipated in the detector is proportional to the breakdown voltage and the avalanche charge; therefore, the charge must be limited to prevent excessive power dissipation, especially in devices with large breakdown voltage. Moreover, it has been recently demonstrated in [8] that the main crosstalk component in SPAD arrays is optical crosstalk: carriers crossing the junction in an avalanche can emit secondary photons that can, in turn, be absorbed by nearby detectors in an array. Minimizing the avalanche charge also minimizes the number of emitted photons, and therefore reduces optical crosstalk. More important still, as the avalanche current flows through the device some of the charge carriers can be captured by trapping centers in the space charge region and released after a random period of time. These carriers can trigger a new avalanche, which in turn can lead to further carrier trapping, and so on; this effect is called afterpulsing. Afterpulsing introduces correlation between consecutive avalanches, and limits the maximum repetition rate. Afterpulsing intensity depends on the type and number of trapping centers present in the device, and also on the amount of charge that flows through the junction during an avalanche. So, reducing the avalanche charge also reduces the afterpulsing probability. The direct integration of a PQC with the detector, therefore, reduces afterpulsing as well.

Another way to reduce afterpulsing intensity is to keep the detector biased below breakdown for a period of time after avalanche quenching. This period is called hold-off time. During hold-off the trapped carriers can be emitted without triggering additional avalanches. Only after the hold-off time is expired the bias voltage is allowed to return to its quiescent value. Unfortunately, the simple passive quenching circuit examined so far is not capable of providing this functionality; however it can be easily modified by additional circuitry, as in [9]. Hold-off time should be adjusted to be long enough to allow trapped carriers to be emitted, but not too long in order not to excessively limit the repetition rate, so a trade-off must be reached.

Another drawback of PQCs is the long reset time. Once the avalanche have been quenched, in fact, the bias voltage slowly returns to its quiescent value with a time constant given by the parasitic capacitance  $C_P$  times the ballast resistor  $R_B$ . The reset

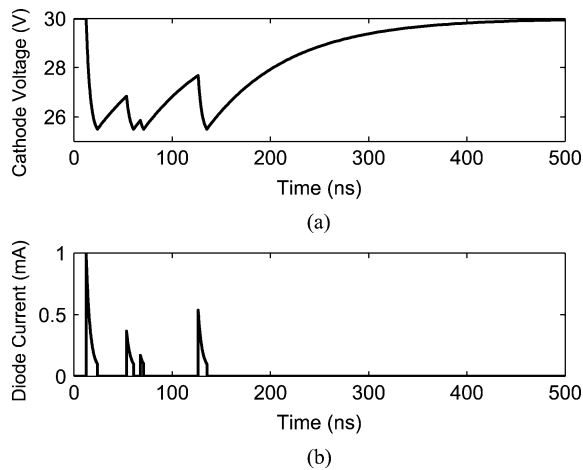


Fig. 5. (a) Cathode voltage and (b) Diode current waveforms for a SPAD connected to a PQC, multiple photon absorption.

time constant can easily be more than two order of magnitude greater than the quench one. For example, for an external PQC the voltage reset time constant, using the values seen so far, would be  $\tau_R = C_P R_B = 1 \mu\text{s}$ , so the voltage reset would take about  $5\tau_R$ , in this case about  $5 \mu\text{s}$ . For PQCs integrated with the detector, however, these times are much smaller: with reference to Fig. 2,  $\tau_R = 100 \text{ ns}$ , and the reset transition lasts about 500 ns. The long exponential reset transition can be seen in Figs. 2 and 5. With reference to [3],  $C_P = 70 \text{ fF}$  and  $R_B = 270 \text{ k}\Omega$ , so the reset time constant is lowered to 18.9 ns. For all the duration of the reset transition, the SPAD bias voltage is above breakdown, so an avalanche can be triggered at any time, but in conditions other than desired. Fig. 5 shows the cathode voltage and diode current waveforms for multiple photon absorption during reset: the current pulses present a smaller amplitude, and are therefore harder to detect. A fast reset is also important because, for avalanches triggered during reset, the diode's performances (in terms of detection efficiency, timing response, etc...) are not only worse than expected, but also variable with time, since the effective bias voltage varies during the whole reset transition. The excess bias voltage is initially so small that the avalanche triggering probability is almost negligible, but it slowly increases to the desired value. When the counting rate becomes greater than the inverse of the reset time, almost all avalanche are triggered during reset, so the bias voltage will not be restored to its quiescent value. At still higher counting rates, a new avalanche is triggered almost immediately after quench, so the bias voltage barely rises above breakdown.

The slow voltage reset causes another effect: for avalanches triggered early during the reset transition, the output pulse may be too small to be detected. The minimum delay that must elapse between two consecutive avalanches in order for both to be detected is called dead time, and in this case may be quite long. Since avalanche triggering is random, the presence of a dead time leads to count losses. There exists methods to correct the count losses [10], [11], but they cannot be applied to PQCs since dead time is not fixed: it depends on the random quenching time and is extended for a further random duration by every

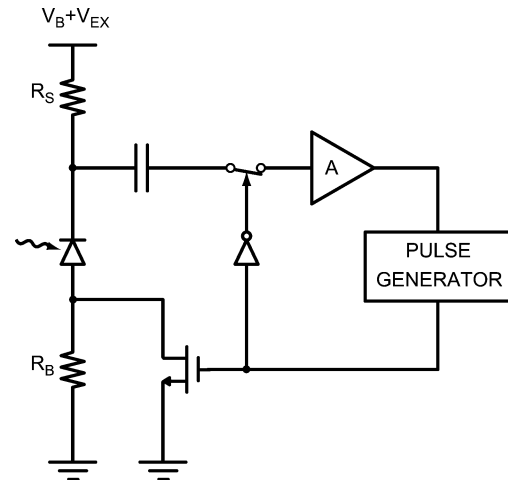


Fig. 6. PQC modified to introduce an Active Reset.

undetected avalanche. This poses a limitation on the maximum counting rate, that must be small compared to the inverse of the full reset time. For an external PQC, since the reset transition is longer, the maximum counting rate is limited to about 10 kcps, as reported in [12]; this figure has been calculated in a way that ensures that the probability of an avalanche being triggered during reset is lower than 1%. Under the same assumptions, for quenching circuits integrated with the detector the counting rate can be higher than 100 kcps. In fact, [13] reports a total dead time of 32 ns and a maximum counting rate of 20 MHz; however, in this case most of the avalanches are triggered during reset, since the reset time constant is reported to be about 30 ns. Using the same calculation criterions as in [12], the limit would be about 133 kcps. Obviously, if the 1% criterion discussed above is discarded, higher counting rates are possible, but always with the order-of—magnitude advantage for integrated PQCs over external ones.

Another way to shorten the reset transition is by adding an active reset circuitry, as in [14] (see Fig. 6). Here the reset transition is fast, in the range of ten nanoseconds. Moreover, the reset command can be delayed to introduce an hold-off time. During hold-off, however, the diode undergoes passive reset, so the hold-off duration is limited: the bias voltage cannot be allowed to rise too much before starting the active reset to prevent avalanche retriggering, so hold-off time is limited to a fraction of the passive reset time constant.

In summary, passive quenching circuits have the drawbacks of presenting a not well defined quenching time, a very slow bias reset (that implies a limited counting rate and the possibility of avalanche triggering during reset) and the impossibility of limiting afterpulsing intensity without resorting to modifications that no longer allow the circuit to be classified as purely passive. The advantages are simplicity, low cost and small area occupation if integrated directly with the detector, allowing the fabrication of large arrays with small loss in fill factor.

Passive quenching circuits are used when small area occupation is required (for example in [15], [16] and [4]) and for characterization purposes (for example in [5], [17], [18] and [19]), and are even commercially available in conjunction with

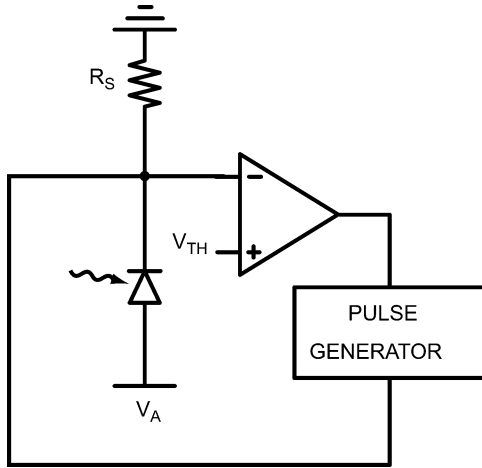


Fig. 7. Basic diagram of an AQC.

SiPMs (Silicon PhotoMultipliers) [20]. The concept of passive quenching circuits has even been used in [21] in studies on avalanche BJTs.

### III. ACTIVE QUENCHING CIRCUITS

To overcome the drawbacks of passive quenching circuits (mainly slow voltage reset and not well defined dead time) a different kind of quenching circuits has been introduced [22]: Active Quenching Circuits (AQC). They were first reported as discrete components circuits in [23], and have even been commercially available as NIM modules [24].

Their operation consists in detecting the avalanche and react back on the device by controlling its bias voltage. The avalanche is sensed through a low impedance, and both quenching and reset are carried out using active components (pulse generators or fast active switches) after which these circuits are named. A basic diagram using a pulse generator as the active circuitry is represented in Fig. 7. Unlike passive quenching circuits, in AQCs the bias voltage is actually lowered below breakdown when quenching an avalanche, so the quenching time is not affected by fluctuations due to the statistical process of avalanche multiplication. After avalanche quenching, the bias voltage is kept below breakdown for a predetermined period (the hold-off time) and then brought back to its quiescent value.

The quenching transition is faster than in PQCs, but the actual quenching time might not be so small. In fact, before an avalanche is quenched, the AQC has to detect the avalanche and intervene. The time taken to do this depends on various factors, such as AQC sensitivity, length of the connection between SPAD and AQC, peak value of the avalanche current (in turn depending on excess bias voltage), and so on. During the wait for the active quenching to take place, the avalanche current keeps on flowing at its peak value, and if the quenching time is too long the total avalanche charge will be high, leading to high power dissipation and high probability of afterpulsing due to trapped charges. The total avalanche charge is given by the peak avalanche current  $I_0$  times the quenching time  $T$ :

$$Q = I_0 T = \frac{V_{EX}}{R_S} T \quad (5)$$

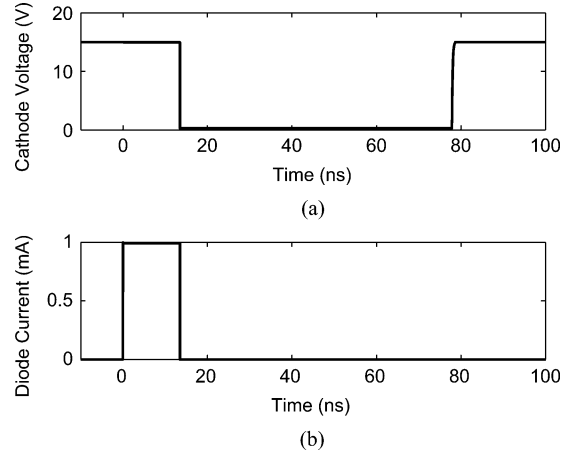


Fig. 8. (a) Cathode voltage and (b) Diode current waveforms for a SPAD connected to an AQC.

so if the quenching time is larger than the passive decay time constant the total charge will be greater than that of PQCs; this happens for

$$T > C_P R_S \left[ 1 + \frac{I_F \ln \left( \frac{I_0 - I_F}{I_S - I_F} \right) - I_S}{I_0} \right] \simeq \tau \alpha. \quad (6)$$

Fig. 8 shows the cathode voltage and diode current waveforms for a SPAD connected to an AQC. The quenching time  $T$  is about 13.5 ns, shorter than the passive quenching time. The avalanche charge is about 13.5 pC, larger than that of PQC. As can be seen, the total avalanche charge does not depend on the parasitic capacitance  $C_P$  but only on the intervention delay. Integration of an AQC with the detector would reduce the total charge anyway, since the shorter connection would entail a shorter propagation delay.

Voltage reset is much faster than in PQCs (from a few nanoseconds to tens of nanoseconds, depending on excess bias voltage and parasitic capacitance), thereby considerably reducing the probability of avalanches occurring during reset. However, active reset is carried out by means of a low impedance device, so avalanches triggered during reset are not sensed until the reset has ended. For avalanches triggered during reset, therefore, the quenching time will be even longer, further increasing the avalanche charge. Given the reset time in the order of ten nanoseconds, the probability of avalanches during reset would be quite small even for count rates up to 1 MHz, so this would not be an issue. In such a case, the probability would be 1%, and the count rates are usually lower than 1 MHz. However, also afterpulsing must be taken into account. Avalanches due to afterpulsing can be triggered as soon as the bias is risen above breakdown. Afterpulsing probability is usually larger than that given above.

The reset duration must then be carefully chosen, so as to be the shortest possible to guarantee full voltage reset. Again, direct integration would reduce the parasitic capacitance, so it would shorten the voltage reset.

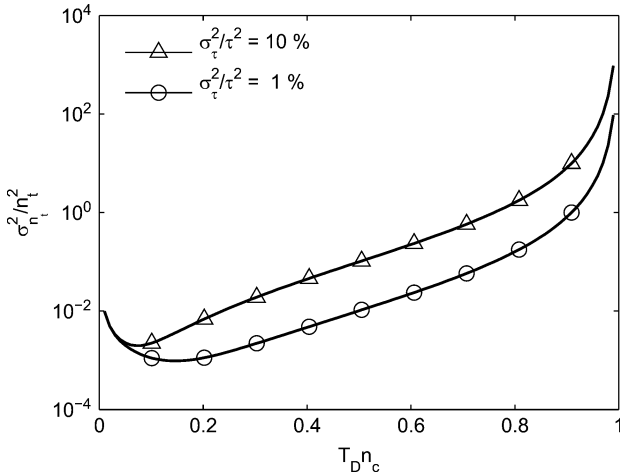


Fig. 9. Relative variance of photon arrival rate estimation as a function of counting rate.

Hold-off time is stable and well defined, since it can be determined by a well-regulated monostable multivibrator. This is important because now dead time correction can be applied to account for photons absorbed during hold-off, when an avalanche cannot be triggered. When the counting rate is low, the difference is negligible. It becomes important, however, for counting rates comparable to the inverse of the dead time. The photon arrival rate can be estimated by [10]:

$$n_p = \frac{n_c}{1 - n_c T_D} \quad (7)$$

where  $n_p$  is the photon arrival rate,  $n_c$  is the measured counting rate and  $T_D$  is the dead time. As can be seen, the estimated rate depends on the dead time  $T_D$ , not only on hold-off time. Therefore it is the dead time that must be known to apply the correction, and the total dead time is given by the sum of quenching delay, hold-off time and voltage reset time. Even a small variation in the total dead time can lead to an inaccurate estimation of photon arrival rate, especially at high counting rates approaching the inverse of the dead time itself. Moreover, uncertainties in the dead time propagate to uncertainties in the photon arrival rate [25]. The relative variance of the estimated photon arrival rate as a function of the relative variance of dead time can be calculated as:

$$\frac{\sigma_{n_p}^2}{n_p^2} = \frac{1}{T_m n_c} + \frac{(T_D n_c)^2}{(1 - T_D n_c)^2} \frac{\sigma_{T_D}^2}{T_D^2} \quad (8)$$

where  $T_m$  is the measure time. A plot of the function is reported in Fig. 9.

It can be easily seen that even for small relative uncertainties in the dead time (1%) the relative uncertainty in the photon arrival rate estimation can become quite large for high counting rates. For most applications, however, the count rate is usually kept low, in order not to have a too large count loss. In these cases, if  $T_D n_c$  is kept below 0.2, the relative variance would be less than 1%, as can be seen in Fig. 9.

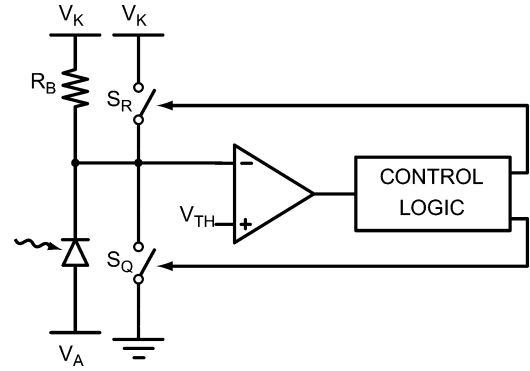


Fig. 10. Basic diagram of a mixed active-passive quenching circuit.

As we have seen, avalanches triggered during voltage reset are quenched with a longer delay, leading to a variation of the dead time and a less accurate estimation of the photon arrival rate. This is a further reason to minimize the reset time, in order to minimize the probability of avalanches triggered during reset. Furthermore, the dead time variation imposes a limit on the maximum applicable dead time correction.

Recapitulating, active quenching circuits offer over PQC's the advantages of faster reset transitions and a well defined and possibly adjustable hold-off time. At the same time they present disadvantages: the avalanche charge (and the afterpulsing probability) depends on the delay of quenching intervention, the circuit is more complex and occupies a larger area. Direct integration of the quenching circuit with the detector would be advantageous, since it would lead to reduced parasitic capacitance, reduced quenching time (since the connection between AQC and SPAD would be very short), reduced avalanche charge, reduced afterpulsing and reduced reset duration. However, the large area of an AQC would reduce the fill factor of detector arrays. To date, no fully integrated purely active quenching circuits has ever been reported, so a full integration with the detector has never been investigated. Purely active AQCs are rarely used at present, except in rare cases [26], [27]. Instead, mixed active-passive quenching circuits are generally preferred.

#### IV. MIXED ACTIVE-PASSIVE QUENCHING CIRCUITS

Mixed active-passive quenching combine the advantages of purely passive and purely active quenching circuits to overcome their respective limitations. The most employed kind of mixed circuits is mixed active-passive quenching with active reset; they were first introduced as discrete components circuits (for example in [28] and [29]) that are still reported at present, see [30]. Also to this class belongs the first ever reported fully integrated non-passive quenching circuit [31]. This class of quenching circuit also benefits from direct integration with the detector thanks to the smaller parasitic capacitance; examples are reported in [32]–[34] and [35].

In this kind of quenching circuits, the SPAD is connected both to a high impedance (usually a large ballast resistor) and to the active quenching and reset circuitry. A basic diagram using switches as the active circuitry is represented in Fig. 10.

When an avalanche is triggered, the avalanche current flows through the ballast resistor, so the avalanche is initially

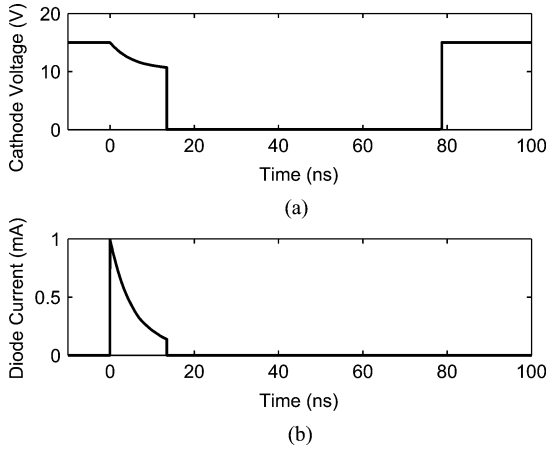


Fig. 11. (a) Cathode voltage and (b) Diode current waveforms for a SPAD connected to a Mixed Active-Passive Quenching Circuit.

quenched like in PQCs. However, the active circuitry soon senses the avalanche and starts the active quenching action. After that, the circuit behaves like an AQC, keeping the SPAD quenched for the hold-off time and then actively restoring the bias voltage. Cathode voltage and diode current waveforms are shown in Fig. 11.

As in PQCs, direct integration of the quenching circuit with the sensor leads to a much reduced parasitic capacitance and therefore to a much smaller avalanche charge, and to a reduced intervention delay; also the voltage reset is faster. However, the integration of both detector and quenching circuit is limited by the area occupation. A typical quenching circuit can measure up to a few  $\text{mm}^2$ , so integration is feasible for single SPADs or small arrays, but not for large arrays.

Compared to PQCs, these quenching circuits offer the advantages of a fast reset and well-defined dead time, exactly like AQCs. Moreover, the total avalanche charge is at most equal to that of PQCs. If the delay of active quenching intervention is too long, the avalanche is passively quenched, so the overall charge equals that of passive quenching circuits; if, however, the delay is shorter, the charge is further limited below this value. The total charge is the integral of the avalanche current from onset until quenching. The quenching time is the minimum between passive quenching threshold crossing (as defined in Section II) and active quenching intervention delay. For the case of shorter active quenching delay  $T$ , i.e., for

$$T < \tau \ln \left( \frac{I_0 - I_F}{I_S - I_F} \right) \quad (9)$$

where  $I_0$ ,  $I_F$ ,  $I_S$  and  $\tau$  are the same as defined in Section II, the avalanche charge can be calculated as:

$$Q = I_F T + (I_0 - I_F) \tau \left( 1 - e^{-T/\tau} \right). \quad (10)$$

With reference to Fig. 11, we have  $T = 13.5$  ns (equal to that of the AQC) and  $Q = 5.1$  pC, less than both AQC and PQC. A comparison of the avalanche charges for the different quenching circuits is shown in Fig. 12. The vertical dashed line indicates the actual active quenching intervention delay (13.5 ns). The

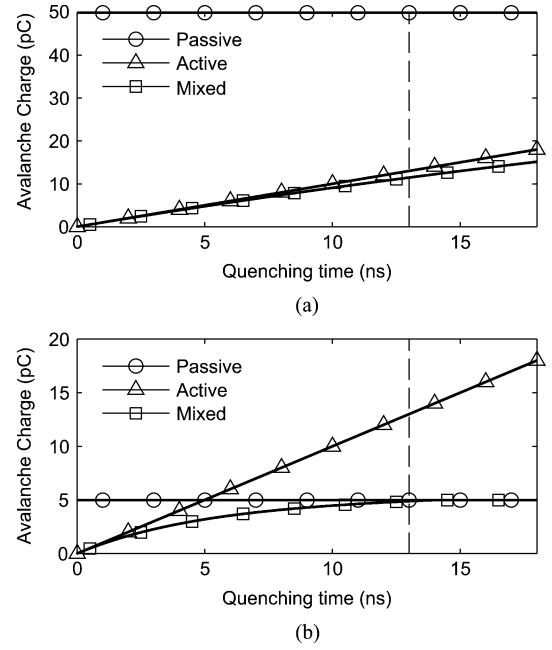


Fig. 12. Comparison among the avalanche charges for different quenching circuits as a function of active quenching intervention delay; (a) External quenching circuit,  $C_P = 10$  pF, (b) Quenching circuits directly integrated with the detector,  $C_P = 1$  pF.

top graph shows the comparison for external quenching circuits. In this case the active quenching time is so much smaller than the passive time constant that there is little difference between the avalanche charges for active and mixed quenching circuits; the mixed quenching circuit is slightly better, however. The charge for the PQC is much larger. The bottom graph shows the comparison for the most recent quenching circuits directly integrated with the detector. As can be seen, for such a small parasitic capacitance, the total avalanche charge for a mixed active-passive quenching circuit is only slightly smaller than that of a PQC, while that of an AQC is much larger.

The main disadvantage of a mixed quenching circuit, compared to a PQC, is the much larger area occupation, that would limit their usage in large and closely packed arrays; however, arrays with small area, simplified mixed active-passive quenching circuits have already been reported, such as [36]. A mixed quenching circuit is still convenient, even with such small parasitic capacitances, because it operates with a fixed and well-regulated dead time and provides an easy way to implement gated operation, that will be described in a later section.

Compared to AQCs, on the other hand, the main advantage is the limitation of the avalanche charge: active quenching delay and peak avalanche current being equal, the avalanche charge in mixed quenching circuits is always smaller than that of AQCs, as can be seen in Fig. 12. There is a drawback, however: in mixed circuits, as well as in purely active circuits, the voltage reset is carried out through a low impedance, so avalanches triggered during reset are not immediately passively quenched, the passive quenching begins after the reset transition has ended. Worst case scenario is that the avalanche is triggered as soon as the bias voltage is brought back over breakdown,

so the peak avalanche current flows through the device for a large fraction of the reset duration. The avalanche charge for these avalanches can easily be more than double that of “conventional” avalanches. It is therefore of the utmost importance to limit the reset to short durations, so as to minimize both the charge of avalanches triggered during reset and the probability of these avalanche being triggered in the first place. Again, direct integration of the quenching circuit with the detector would greatly help in decreasing the reset duration. With regard to dead time correction, mixed active-passive quenching circuits present the same caveats as purely active circuits, namely variations of the dead time due to avalanches triggered during reset.

Other combinations of passive and active operation are possible as well: a simple example, already mentioned in Section II [14], is passive quenching with active reset. Here the quenching is always passive, so the avalanche charge is that of PQC; the reset is active, with all the advantages and disadvantages already examined. Moreover, hold-off time is limited to a fraction of the passive reset time constant. This circuit has been further developed as reported in [37]. Another recent example is [38], where the avalanche is quenched thanks to the large ‘off’ resistance of MOS transistors, while the bias voltage is reset through a different MOS transistor. A similar technique is used in [39].

Another possibility is that of active quenching and passive reset (used, for example, in [9], [40]), although this class of circuits would present all the disadvantages of AQC (quenching delay may be too long) and PQC (reset transition too slow). Here, however, the ballast resistor is not meant to quench the avalanche, so it can have a smaller value. This way, the reset time constant would be smaller, and the reset transition faster, than that of PQC; for example [30] reports reset times of a few nanoseconds. The main advantage in doing this is the lack of overshoots and ringing at the end of the reset transition. Another way to reduce overshoots at the end of the voltage reset is to substitute the ballast resistor with an active load as reported in [41]. In this circuit, the active load is essentially a current mirror, where the output current and the output impedance are chosen to guarantee that passive quenching takes place. At the reset end, however, the output transistor is biased in the ohmic region, thus ensuring a low impedance path to the power supply, and this ensures that overshoots and ringing are dampened.

A different approach is demonstrated in [42]. Here the topology is the same as that of mixed active-passive quenching circuits, but instead of the ballast resistor there is an MOS transistor for easier integration. The SPAD’s anode terminal is connected to an inverter acting as a voltage comparator, and two more transistor constitute the quench and reset circuitry. However, the gate bias voltage of the ballast MOS can be varied, in order to lower its output resistance and transform the circuit into a purely active quenching circuit. This way, the same circuit could be used in two different ways, thus allowing to compare the performances of the two approaches, purely active versus mixed active-passive. The authors, however, do not offer any figure on this comparison, since that was not the purpose of their paper.

In summary, mixed active-passive quenching circuits improve on the operation of both purely passive and purely active

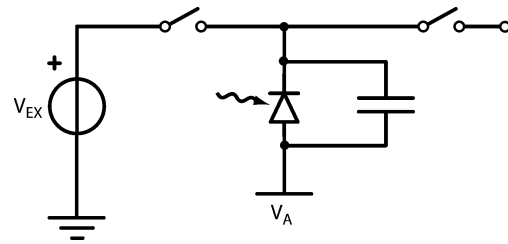


Fig. 13. Basic diagram of the DigitalAPD quenching circuit.

quenching circuits, and are widely employed in literature, both integrated with the detector [35], [36] and as separate ICs [41], [43], [44]. As separate ICs, mixed quenching circuits are used in commercially available photon detection modules [45], [46].

## V. DIFFERENT QUENCHING CIRCUITS

Other than traditional purely passive, purely active and mixed active-passive quenching circuits, other circuit topologies have been reported in literature. All this circuits are intended to be integrated with the detector in order to take advantage of the smaller parasitic capacitance and the smaller propagation delay.

A first examples is reported in [47], where a bidimensional detector array is proposed. A basic diagram is shown in Fig. 13. The authors chose to avoid active quenching circuits in order to obtain a densely packed array (since typical AQC take up a large silicon area compared to the detector), and passive quenching circuits as well to allow high count rates. Instead they opted for a novel quenching mechanism, although still based on passive quenching and gating, that they call DigitalAPD. The authors take advantage of the parasitic capacitance of the detectors to operate the devices in a manner similar to a dynamic RAM. The parasitic capacitance is charged to the full bias voltage above breakdown and left floating for the whole gate-on period, and after that the capacitance is again discharged. If an avalanche is triggered during the gate-on period, the avalanche current discharges the parasitic capacitance, so the total avalanche charge is limited by that stored in the capacitance. This behavior is indeed that of a passive quenching circuit with a very large ballast resistor, in this case the switches’ ‘off’ resistance. At the end of the gate-on period, the bias voltage is brought back to below breakdown, thereby discharging the capacitance and quenching any still-active avalanche. This concept has the advantage of a very small area occupation, since the only other elements besides the detectors are switches, and thus it can easily be used in large arrays with good fill factor. However, the circuit suffers from several drawbacks such as limited gate-on times and charge sharing issues similar to those present in DRAMs, since the detector capacitance is small and at readout the stored charge can be disrupted by charge sharing; this must be kept in mind when designing arrays since it poses a size limitation. Further developments on this concept have not been reported since.

In [48], the authors present a thyristor-based dynamic quenching circuit (see Fig. 14). Here, in quiescent state, the circuit takes advantage of the different sizing of the transistors ( $M_2$  bigger than  $M_1$ , and  $M_3$  bigger than  $M_4$ ) and, consequently, their different leakage currents to properly keep the

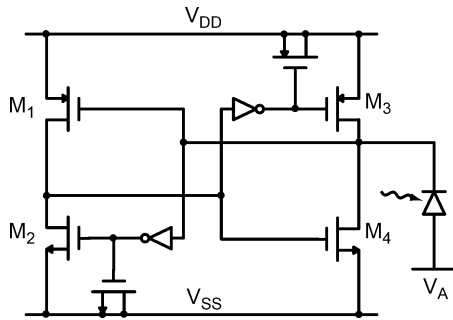


Fig. 14. Basic diagram of the thyristor-based dynamic quenching circuit.

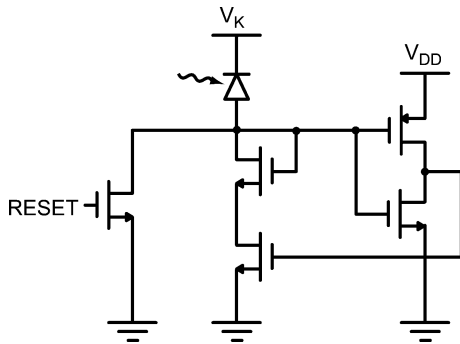


Fig. 15. Basic diagram of the current-mode quenching circuit.

SPAD cathode biased to the positive power supply  $V_{DD}$ . When an avalanche is triggered, the high impedance at the cathode node starts a passive quenching action, but immediately  $M_1$  and  $M_4$  are turned on to bring the cathode voltage to  $V_{SS}$ . After a propagation delay, given by the inverters and the two MOS transistors used as capacitors, the two remaining transistors turn on as well, overpowering  $M_1$  and  $M_4$  and resetting the cathode voltage. As stated in [48], the circuit can easily be modified to provide an adjustable hold-off time. The circuit presents a small area occupation,  $130 \mu\text{m}^2$  as stated by the authors, and is intended for integration of large arrays. Very fast operation is reported: the shortest cited quench duration is 2 ns, and the power dissipation is  $60 \mu\text{W}$  at 25 MHz firing range. However, all reported results are based on simulations only.

In [49], the authors propose a current-mode quenching circuit (see Fig. 15). In this circuit, the avalanche current is sensed through a current mirror and used to increase the resistance of, and eventually turn off, a transistor connected in series to the SPAD. This way, the current flow is interrupted, and the avalanche quenched in a manner similar to the previous circuit. The ballast resistance, however, increases during the quenching action instead of always being very large, and this implies a slower avalanche quenching. Since current-mode circuits are usually faster than their voltage-mode counterparts, the proposed circuit should provide faster quench and reset times. Moreover, the circuit uses only a few transistors, and thus occupies a small silicon area. It would easily be possible to integrate the circuit together with the detector. However, the authors provide only simulation results and measurements obtained with the use of discrete devices, despite having presented the same topology for several years now without ever producing a fully integrated circuit.

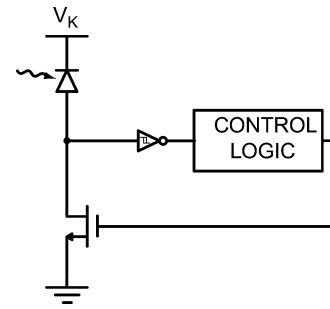


Fig. 16. Basic diagram of the variable-load quenching circuit.

A similar concept is proposed in [50] (Fig. 16). Here, too, the quenching element is a transistor with variable channel resistance, but the avalanche is sensed by a voltage comparator. The operating condition of the load transistor is adjusted over time: it is kept in the linear region in quiescence (to correctly bias the SPAD), enters the saturation region in the initial phase of the avalanche (thus limiting the avalanche current), is then turned off to present a high impedance for avalanche quenching (and kept off for the whole hold-off period), and finally turned on again to reset the detector bias to quiescent conditions. Like all the quenching circuits directly integrated together with the sensor, this design has the advantage of minimizing the parasitic capacitance on the detector terminals, and hence the avalanche charge. Although the occupied area is not as small as that of [47], large arrays can still be fabricated with good fill factor. Moreover, each cell contains the whole quenching circuit with a digital output and each detector is handled independently, so there are no charge sharing issues that limit the array size. A  $32 \times 32$  array based on this concept has already been reported [51].

## VI. GATED OPERATION

All the quenching circuits examined until now operate in the so-called free-running mode of operation. In this mode, the detector is always biased above breakdown at a fixed voltage. This way, the SPAD is always ready to detect photons. There exist situations, however, where this mode of operation is not the most suitable. For example in laser ranging [52], OTDR (Optical Time-Domain Reflectometry) [53], laser induced fluorescence [54] and QKD (Quantum Key Distribution) [55], the signal to be detected originates from a single laser pulse. In these cases, the signal is present only in a well defined interval after the laser pulse, so it can be convenient to enable the detector only in this time interval. Moreover, in the case of laser induced fluorescence, the laser pulse can be so intense as to completely drown out the signal. Again, the diode can be kept inactive in the presence of the laser pulse, and reactivated immediately afterwards. This mode of operation is called gated mode, and consists in keeping the bias voltage below breakdown, and increasing it at the desired level for a well defined period of time coincident with the expected signal arrival. In most applications the gate-on time is usually kept short (even down to less than a nanosecond, as in QKD [56]), but some applications, such as digital lock-in techniques [57] or non-invasive optical testing of VLSI circuits [58], require much longer gate-on times.

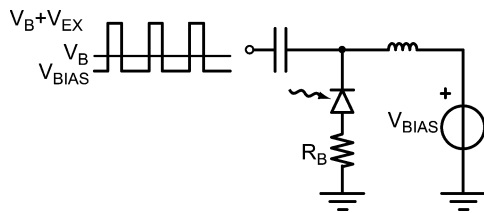


Fig. 17. Basic diagram of SPAD gated operation using a bias-tee.

When the gate-on time is short, any avalanche will be quenched when the bias voltage is lowered at gate termination. In this case it is not necessary to employ quenching circuits. In fact, if an active quenching circuit was used, the reaction time could even be longer than the total gate time. On the other hand, a PQC's large ballast resistor could prevent fast transitions at the beginning and end of the gating period (see, for example, [59]). Obviously, if there is no mechanism to quench an avalanche and restore the device bias, only a single photon can be detected for each gate period, but that is the purpose of having a short gate-on time in the first place. If the gate-on time is longer, avalanche quenching by gate termination may not guarantee that the overall avalanche charge be kept small, and it would therefore be necessary to add an additional quenching mechanism, either passive or active.

In the case of passive circuits, the gating pulse is usually applied through AC coupling, often using a bias-tee, since in DC coupling the large ballast resistor, together with the detector's parasitic capacitance, would form a low-pass filter that would significantly slow down the pulse edges. Using AC coupling, on the other hand, the pulse is applied through an high-pass filter, so the pulse edges would not be modified. The high-pass filtering, however, imposes a limitation on the maximum pulse duration, in order to keep the bias voltage from changing too much during the gating pulse. Moreover, the coupling capacitor cannot be too small. In that case, the actual voltage pulse would be reduced by capacitive voltage division between the coupling capacitor and the detector's parasitic capacitance. It is therefore necessary to employ a discrete capacitor instead of an integrated one; also well known is the difficulty of integrating inductors. The repetition rate is also limited by the coupling capacitor recharge time constant. A basic schematic of SPAD gated operation using a bias-tee is shown in Fig. 17.

Other circuits have been reported to overcome this drawbacks, for example that reported in [60], where AC coupling is used in conjunction with diodes to limit the recharge time constant. Moreover, the avalanche current flows only through the coupling capacitor, so the overall avalanche charge is limited to that stored in the capacitor. Taking into account the capacitive voltage division, the coupling capacitor can be kept small, so the charge will be small as well. The capacitor may not be small enough, however, to allow easy integration.

A different approach is sinusoidal gating, as reported in [61]. Here, the bias voltage is changed using a high-frequency sinusoidal voltage, with peaks coincident with the estimated photon arrival. This way, the gate-on times can be kept very short, in the nanosecond range, and the gating signal can be easily filtered without degrading the avalanche pulses.

If the gate-on time is very long, much longer than the quench and recharge time, passive quenching can still be employed, but it would present the same drawbacks as passive quenching circuits in free running mode.

With regard to active and mixed quenching circuits, they are easily adaptable to accommodate gating operation. The gating signal can be used to drive the quenching switch, for example by simply connecting the active quenching command and the gate command to the inputs of an OR gate, and driving the switch with its output. Moreover, there are no limitations on gate-on or gate-off duration, nor on repetition rate, except for very short times, shorter than the minimum duration required to swing the voltages to the desired values. For an example of gated operation of a mixed active-passive quenching circuit, see [62] or [63]. In this example the quenching circuit is external, since it is fabricated in a standard CMOS process and is used in conjunction with an InGaAs detector, but similar techniques can be easily employed for a mixed quenching circuit integrated with the detector.

## VII. CONCLUSION

In this paper different kinds of quenching circuits have been examined, with particular attention to the advantages of direct integration with the SPAD detector. The main advantages are related to the much reduced parasitic capacitance, which leads to reduced avalanche charge, reduced quenching time and reduced afterpulsing. Attention must be paid to the area occupation: with some of the quenching circuits examined this would prevent the integration of large or closely packed detector arrays.

## REFERENCES

- [1] C. Niclass, M. Gersbach, R. Henderson, L. Grant, and E. Charbon, "A single photon avalanche diode implemented in 130-nm CMOS technology," *IEEE J. Sel. Topics Quantum Electron.*, vol. 13, no. 4, pp. 863–869, Jul./Aug. 2007.
- [2] A. D. Mora, A. Tosi, S. Tisa, and F. Zappa, "Single-photon avalanche diode model for circuit simulations," *IEEE Photon. Technol. Lett.*, vol. 19, pp. 1922–1924, Dec. 2007.
- [3] C. Niclass, A. Rochas, P.-A. Besse, and E. Charbon, "Toward a 3-D camera based on single photon avalanche diodes," *IEEE J. Sel. Topics Quantum Electron.*, vol. 10, no. 4, pp. 796–802, Jul./Aug. 2004.
- [4] S. Bellis, J. C. Jackson, and A. Mathewson, "Towards a disposable in vivo miniature implantable fluorescence detector," in *Society of Photo-Optical Instrumentation Engineers (SPIE) Conference Series*, Mar. 2006, vol. 6083, pp. 140–147.
- [5] J. Hu, X. Xin, X. Li, J. Zhao, B. VanMil, K.-K. Lew, R. Myers-Ward, C. Eddy, and D. Gaskill, "4H-SiC visible-blind single-photon avalanche diode for ultraviolet detection at 280 and 350 nm," *IEEE Trans. Electron Devices*, vol. 55, pp. 1977–1983, Aug. 2008.
- [6] C. Niclass, A. Rochas, P.-A. Besse, R. Popovic, and E. Charbon, "A 4  $\mu$ s integration time imager based on CMOS single photon avalanche diode technology," *Sensors and Actuators A: Physical*, vol. 130–131, pp. 273–281, 2006.
- [7] J. Šíp and O. Wilfert, "Quenching circuit for single-photon quantum key distribution," *Proceedings of Radioelektronika*, pp. 253–256, 2004.
- [8] I. Rech, A. Ingargiola, R. Spinelli, I. Labanca, S. Marangoni, M. Ghioni, and S. Cova, "Optical crosstalk in single photon avalanche diode arrays: A new complete model," *Opt. Express*, vol. 16, no. 12, pp. 8381–8394, 2008.
- [9] R. G. W. Brown, R. Jones, J. G. Rarity, and K. D. Ridley, "Characterization of silicon avalanche photodiodes for photon correlation measurements. 2: Active quenching," *Appl. Opt.*, vol. 26, no. 12, pp. 2383–2389, 1987.
- [10] J. W. Müller, "Dead-time problems," *Nuclear Instruments and Methods*, vol. 112, no. 1-2, pp. 47–57, 1973.

- [11] S. Pommé, "Time-interval distributions and counting statistics with a non-paralysable spectrometer," *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 437, no. 2-3, pp. 481–489, 1999.
- [12] S. Cova, M. Ghioni, A. Lacaita, C. Samori, and F. Zappa, "Avalanche photodiodes and quenching circuits for single-photon detection," *Applied Optics*, vol. 35, pp. 1956–1976, Apr. 1996.
- [13] A. Rochas, M. Gosch, A. Serov, P. Besse, R. Popovic, T. Lasser, and R. Rigler, "First fully integrated 2-D array of single-photon detectors in standard CMOS technology," *IEEE Photon. Technol. Lett.*, vol. 15, pp. 963–965, Jul. 2003.
- [14] M. Liu, C. Hu, J. Campbell, Z. Pan, and M. Tashima, "Reduce afterpulsing of single photon avalanche diodes using passive quenching with active reset," *IEEE J. Quantum Electron.*, vol. 44, pp. 430–434, May 2008.
- [15] M. Marwick and A. Andreou, "Single photon avalanche photodetector with integrated quenching fabricated in TSMC 0.18  $\mu\text{m}$  1.8 V CMOS process," *Electronics Letters*, vol. 44, no. 10, pp. 643–644, 2008.
- [16] J. Richardson, L. Grant, and R. Henderson, "Low dark count single-photon avalanche diode structure compatible with standard nanometer scale CMOS technology," *IEEE Photon. Technol. Lett.*, vol. 21, pp. 1020–1022, Jul. 2009.
- [17] Y.-S. Kim, V. Makarov, Y.-C. Jeong, and Y.-H. Kim, "Silicon single-photon detector with 5 Hz dark counts," in *Lasers and Electro-Optics, 2009 and 2009 Conference on Quantum Electronics and Laser Science Conference. CLEO/QELS 2009*, 2–4, 2009, pp. 1–2.
- [18] R. E. Warburton, M. Itzler, and G. S. Buller, "Free-running, room temperature operation of an InGaAs/InP single-photon avalanche diode," *Applied Physics Letters*, vol. 94, no. 7, p. 071116, 2009.
- [19] B. Nouri, M. Dandin, and P. Abshire, "Characterization of single-photon avalanche diodes in standard CMOS," *Sensors, 2009 IEEE*, pp. 1889–1892, 2009.
- [20] SensL 2009 [Online]. Available: <http://www.sensl.com/>
- [21] R. Popovic and M. Lany, "Counting single electrons in a CMOS circuit," in *Microelectronics, 2008. MIEL 2008. 26th International Conference*, May 2008, pp. 55–60.
- [22] P. Antognetti, S. Cova, and A. Longoni, "A study of the operation and performances of an avalanche diode as a single photon detector," in *2nd ISRA Nuclear Electronic Symposium*, May 20–23, 1975.
- [23] S. Cova, A. Longoni, and G. Ripamonti, "Active-quenching and gating circuits for single-photon avalanche diodes (SPADs)," *IEEE Trans. Nucl. Sci.*, vol. 29, pp. 599–601, Feb. 1982.
- [24] S. Cova, "Active Quenching Circuit for Avalanche Photodiodes," U.S. patent 4,963,727, Oct. 20, 1990, (Italian patent 22367A/88); licensed for industrial production to Silena SpA, Milano, Italy.
- [25] D. F. Yu and J. A. Fessler, "Mean and variance of singles photon counting with deadline," *Med. Biol.*, vol. 45, pp. 2043–2056, 2000.
- [26] I. Prochazka, K. Hamal, and L. Kral, "Single photon counting module for space applications," *Journal of Modern Optics*, vol. 54, no. 2 & 3, pp. 151–161, Jan. 2007.
- [27] T. Frach, G. Prescher, C. Degenhardt, R. de Gruyter, A. Schmitz, and R. Ballizany, "The digital silicon photomultiplier—principle of operation and intrinsic detector performance," in *Nuclear Science Symposium Conference Record (NSS/MIC), 2009 IEEE*, Oct. 2009, pp. 1959–1965.
- [28] H. Dautet, P. Deschamps, B. Dion, A. D. MacGregor, D. MacSween, R. J. McIntyre, C. Trottier, and P. P. Webb, "Photon counting techniques with silicon avalanche photodiodes," *Appl. Opt.*, vol. 32, no. 21, pp. 3894–3900, 1993.
- [29] M. Ghioni, S. Cova, F. Zappa, and C. Samori, "Compact active quenching circuit for fast photon counting with avalanche photodiodes," *Review of Scientific Instruments*, vol. 67, no. 10, pp. 3440–3448, 1996.
- [30] M. Stipcevic, "Active quenching circuit for single-photon detection with Geiger mode avalanche photodiodes," *Appl. Opt.*, vol. 48, no. 9, pp. 1705–1714, 2009.
- [31] F. Zappa, A. Lotito, A. Giudice, S. Cova, and M. Ghioni, "Monolithic active-quenching and active-reset circuit for single-photon avalanche detectors," *IEEE J. Solid-State Circuits*, vol. 38, pp. 1298–1301, Jul. 2003.
- [32] F. Zappa, S. Tisa, A. Gulinatti, A. Gallivanoni, and S. Cova, "Complete single-photon counting and timing module in a microchip," *Opt. Lett.*, vol. 30, no. 11, pp. 1327–1329, 2005.
- [33] D. Stoppa, D. Mosconi, L. Pancheri, and L. Gonzo, "Single-photon avalanche diode CMOS sensor for time-resolved fluorescence measurements," *IEEE Sensors J.*, vol. 9, pp. 1084–1090, Sep. 2009.
- [34] S. Tisa, A. Tosi, and F. Zappa, "Fully-integrated CMOS single photon counter," *Optics Express*, vol. 15, no. 6, pp. 2873–2887, 2007.
- [35] H. Finkelstein, M. J. Hsu, S. Zlatanovic, and S. Esener, "Performance trade-offs in single-photon avalanche diode miniaturization," *Review of Scientific Instruments*, vol. 78, no. 10, p. 103, Oct. 2007.
- [36] D. Mosconi, D. Stoppa, L. Pancheri, L. Gonzo, and A. Simoni, "CMOS single-photon avalanche diode array for time-resolved fluorescence detection," in *Solid-State Circuits Conference, 2006. ESSCIRC 2006. Proceedings of the 32nd European*, Sep. 2006, pp. 564–567.
- [37] C. Hu, M. Liu, X. Zheng, and J. Campbell, "Dynamic range of passive quenching active reset circuit for single photon avalanche diodes," *IEEE J. Quantum Electron.*, vol. 46, pp. 35–39, Jan. 2010.
- [38] M. Grönholm, J. Poikonen, and M. Laiho, "A ring-oscillator-based active quenching and active recharge circuit for single photon avalanche diodes," in *Circuit Theory and Design, 2009. ECCTD 2009. European Conference*, 23–27, 2009, pp. 5–8.
- [39] C. Niclass, C. Favi, T. Kluter, M. Gersbach, and E. Charbon, "A  $128 \times 128$  single-photon image sensor with column-level 10-Bit time-to-Digital converter array," *IEEE J. Solid-State Circuits*, vol. 43, pp. 2977–2989, Dec. 2008.
- [40] R. G. W. Brown and M. Daniels, "Characterization of silicon avalanche photodiodes for photon correlation measurements. 3: Sub-Geiger operation," *Appl. Opt.*, vol. 28, no. 21, pp. 4616–4621, 1989.
- [41] A. Gallivanoni, I. Rech, D. Resnati, M. Ghioni, and S. Cova, "Monolithic active quenching and picosecond timing circuit suitable for large-area single-photon avalanche diodes," *Optics Express*, vol. 14, no. 12, pp. 5021–5030, 2006.
- [42] L. Pancheri and D. Stoppa, "A SPAD-Based pixel linear array for high-speed time-gated fluorescence lifetime imaging," in *ESSCIRC '09*, 2009, pp. 428–431.
- [43] A. Rochas, C. Guillaume-Gentil, J.-D. Gautier, A. Pauchard, G. Ribordy, H. Zbinden, Y. Leblebici, and L. Monat, "ASIC for high-speed—gating and free running operation of SPADs," *Photon Counting Applications, Quantum Optics, and Quantum Cryptography, Proceedings of the SPIE*, vol. 6583, 2007.
- [44] R. T. Thew, D. Stucki, J.-D. Gautier, A. Rochas, and H. Zbinden, "Free-running InGaAs/InP avalanche photodiode with active quenching for single photon counting at telecom wavelengths," *Applied Physics Letters*, vol. 91, p. 201114, 2007.
- [45] Micro Photon Devices, 2009 [Online]. Available: <http://www.microphotondevices.com/>
- [46] Id Quantique, 2009 [Online]. Available: <http://www.idquantique.com/>
- [47] S. Bellis, R. Wilcock, and C. Jackson, M. M. Blouke, Ed., "Photon counting imaging: The digitalAPD," in *Society of Photo-Optical Instrumentation Engineers (SPIE) Conference Series*, Feb. 2006, vol. 6068, pp. 111–120.
- [48] J. Richardson, R. K. Henderson, and D. Renshaw, "Dynamic quenching for single photon avalanche diode arrays," in *Proceedings of 2007 International Image Sensor Workshop*, 2007.
- [49] R. Mita and G. Palumbo, "High-speed and compact quenching circuit for single-photon avalanche diodes," *IEEE Trans. Instrum. Meas.*, vol. 57, pp. 543–547, Mar. 2008.
- [50] S. Tisa, F. Guerrieri, and F. Zappa, "Variable-load quenching circuit for single-photon avalanche diodes," *Optics Express*, vol. 16, no. 3, pp. 2232–2244, 2008.
- [51] F. Guerrieri, S. Tisa, and F. Zappa, "Fast single-photon imager acquires 1024 pixels at 100 kframe/s," *Proceedings of SPIE*, vol. 7249, no. 72490U, 2009.
- [52] M. Pfennigbauer and A. Ullrich, "Applicability of single photon detection for laser radar," *E & I Elektrotechnik und Informationstechnik*, vol. 124, no. 6, pp. 180–185, unpublished.
- [53] M. Tateda and T. Horiguchi, "Advances in optical time-domain reflectometry," *Lightwave Technology*, vol. 7, no. 8, pp. 1217–1224, Aug. 1989.
- [54] J. R. Lakowicz, *Principles of Fluorescence Spectroscopy*, Third ed. Norwell, MA: Kluwer Academic/Plenum Publishers, 2006.
- [55] H. Zbinden, H. Bechmann-Pasquinucci, N. Gisin, and G. Ribordy, "Quantum cryptography," *Applied Physics B: Lasers and Optics*, vol. 67, no. 6, pp. 743–748.
- [56] A. Restelli, J. C. Bienfang, C. W. Clark, I. Rech, I. Labanca, M. Ghioni, and S. Cova, "Improved timing resolution single-photon detectors in daytime free-space quantum key distribution with 1.25 GHz transmission rate," *Selected Topics in Quantum Electronics, IEEE*, vol. PP, no. 99, pp. 1–7, 2010.
- [57] S. Cova, A. Longoni, and I. Freitas, "Versatile digital lock-in detection technique: Application to spectrofluorometry and other fields," *Review of Scientific Instruments*, vol. 50, no. 3, pp. 296–301, 1979.

- [58] F. Stellari, A. Tosi, F. Zappa, and S. Cova, "CMOS circuit testing via time-resolved luminescence measurements and simulations," *IEEE Trans. Instrum. Meas.*, vol. 53, pp. 163–169, Feb. 2004.
- [59] A. D. Mora, A. Tosi, F. Zappa, S. Cova, D. Contini, A. Pifferi, L. Spinelli, A. Torricelli, and R. Cubeddu, "Fast-gated single-photon avalanche diode for wide dynamic range near infrared spectroscopy," *IEEE J. Sel. Topics Quantum Electron.*, vol. PP, no. 99, pp. 1–8, 2010.
- [60] S. Dimler, J. Ng, R. Tozer, G. Rees, and J. David, "Capacitive quenching measurement circuit for Geiger-mode avalanche photodiodes," *IEEE J. Sel. Topics Quantum Electron.*, vol. 13, no. 4, pp. 919–925, Jul./Aug. 2007.
- [61] N. Namekata, S. Sasamori, and S. Inoue, "800 MHz single-photon detection at 1550-nm using an InGaAs/InP avalanche photodiode operated with a sinusoidal gating," in *Optical Communications, 2006. ECOC 2006. European Conference*, 24–28, 2006, pp. 1–2.
- [62] A. Tosi, A. Gallivanoni, F. Zappa, and S. Cova, "Gated operation of InGaAs SPADs with active quenching and fast timing circuits," in *Proceedings of SPIE Optics East 2006*, W. Becker, Ed. Philadelphia, PA: SPIE, 2006, vol. 6372, p. 63720Q.
- [63] J. Zhang, R. Thew, J.-D. Gautier, N. Gisin, and H. Zbinden, "Comprehensive characterization of InGaAs-InP avalanche photodiodes at 1550 nm withn active quenching ASIC," *IEEE J. Quantum Electron.*, vol. 45, pp. 792–799, Jul. 2009.