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A Spartan 6 FPGA-based data acquisition system for dedicated imagers in nuclear medicine*

E Fysikopoulos[1,2], G Loudos[2], M Georgiou[2,3], S David[2] and G Matsopoulos[1]

[1] School of Electrical and Computer Engineering, National Technical University of Athens, Athens, Greece
[2] Department of Medical Instruments Technology, Technological Educational Institute of Athens, Athens, Greece
[3] Department of Nuclear Medicine, Medical School, University of Thessaly, Larissa, Greece

E-mail: lefteris.fysikopoulos@gmail.com

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Abstract
We present the development of a four-channel low-cost hardware system for data acquisition, with application in dedicated nuclear medicine imagers. A 12 bit octal channel high-speed analogue to digital converter, with up to 65 Msps sampling rate, was used for the digitization of analogue signals. The digitized data are fed into a field programmable gate array (FPGA), which contains an interface to a bank of double data rate 2 (DDR2)-type memory. The FPGA processes the digitized data and stores the results into the DDR2. An ethernet link was used for data transmission to a personal computer. The embedded system was designed using Xilinx's embedded development kit (EDK) and was based on Xilinx's Microblaze soft-core processor. The system has been evaluated using two different discrete optical detector arrays (a position-sensitive photomultiplier tube and a silicon photomultiplier) with two different pixelated scintillator arrays (BGO, LSO:Ce). The energy resolution for both detectors was approximately 25%. A clear identification of all crystal elements was achieved in all cases. The data rate of the system with this implementation can reach 60 Mbits s^{-1}. The results have shown that this FPGA data acquisition system is a compact and flexible solution for single-photon-detection applications.

Keywords: field programmable gate array (FPGA), position-sensitive photomultiplier tube (PSPMT), silicon photomultiplier (SiPM), embedded development kit (EDK), data acquisition (DAQ)

1. Introduction

In recent decades, there has been a great interest in nuclear medicine, whose main applications are in the field of oncology, but are continuously extended. While most medical imaging techniques provide anatomical information on structures inside the body, nuclear medicine provides functional information, which is useful for the detection of tumors at early stages, as well as imaging other metabolic processes. Depending on the type of the radioisotope labeling, nuclear medicine techniques can be split into single-photon detection or coincidence detection. The main parts of a nuclear imaging system are the scintillator, the optical detector, the front-end electronics and the data acquisition system [1]. In the case of coincidence detection methods, there is need for fast scintillators and optical detectors. A position-sensitive photomultiplier tube (PSPMT) is by far the most popular optical detector used in such systems. Recently, there has been great interest in a silicon photomultiplier (SiPM)

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as an alternative optical detector due to its fast response. Consequently, there is a need for data acquisition systems that support high digitization and processing rates.

The current trend is the replacement of analogue processing of the scintillation pulse by its digital equivalent implemented on a field programmable gate array (FPGA). A number of groups have already used FPGAs along with high-speed analogue to digital converters (ADCs) as a part of their data acquisition system for signal digitization and/or processing [2–5]. As programmable technology grows fast, different architectures using recently developed standards can be used for various applications in nuclear medicine.

A new data acquisition system has been developed with application in dedicated imagers for small animals and/or human organs based on PSPMTs and SiPM optical detectors. This work was motivated by the evolving need for compact, low-cost, flexible and high data rate data acquisition systems. It is based on high-speed, low-consumption amplifiers and analogue to digital converters (ADCs) connected to an FPGA for processing and transmission of the digitized data to a personal computer (PC). The use of mezzanine standard (FMC) for ADC connection to the FPGA leads to a modular architecture. In this paper, we describe the hardware requirements as well as the implementation of the embedded system based on the combination of ADC/FPGA/DDR technologies which offer high data rate storage of the events of interest.

2. Materials and methods

2.1. System overview

2.1.1. Gamma detector and front-end electronics. Two different systems were used for the validation of the current implementation.

Imaging gamma probe based on a Hamamatsu R8900U-00-C12 PSPMT. A pixelated BGO scintillator array with a crystal element of size $2 \times 2 \times 5\,\text{mm}^3$ and 2.3 mm pitch was coupled to the PSPMT without any optical diffuser. The optimal high voltage was set to −850 V for 511 keV excitation. The PSPMT has 12 anode outputs, six for the x coordinate and six for the y coordinate, which are reduced to two $\overline{X}$ and two $\overline{Y}$ position signals using a standard resistive chain. Four custom pre-amplifiers at the end of the resistive chain shape the signals, taking into account the ADC sampling rate [6].

Imaging gamma probe based on SensL's SiPM array. A SensL's scalable SiPM array (SPMArray4) is a commercially available, solid-state, large array detector based on SiPM technology [7]. It consists of 16 pixel elements covering an active area of $13.6\,\text{mm}^2$. Each pixel has 3640 microcells connected in parallel, with individual cell dimensions equal to 35 μm. The particular SPMArray4 detector has been programmed to the optimum bias voltage of +29.3 V by the manufacturer. Two different pixelated scintillator arrays were coupled to the SiPM array: (a) BGO with $2 \times 2 \times 5\,\text{mm}^3$ pixel size and 2.3 mm pitch, (b) LSO:Ce with $2 \times 2 \times 15\,\text{mm}^3$ pixel size and 2.5 mm pitch. The SensL SPMArray4-A0 pre-amplification electronics and an SPMArray4-A1 evaluation board that provides the pixels voltage output were used in this study. The pre-amplification board mainly consists of 16 differential fast amplifiers (AD8132). The evaluation board provides 16 individual pixel voltage outputs, plus one more output which is the sum signal. The 16 outputs are reduced to two $\overline{X}$ and two $\overline{Y}$ position signals through a symmetric division circuit, first introduced by Popov *et al* [8]. More information about this system can be found in [9].

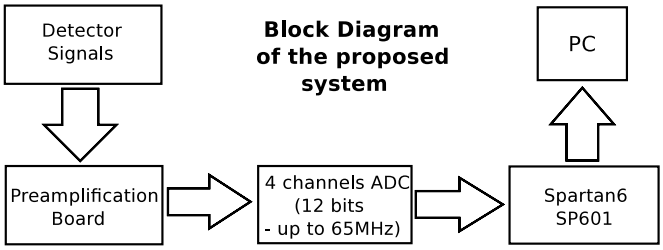


Figure 1. High-level architecture of the proposed system.

2.1.2. The acquisition board. In order to perform sampling, a 12 bit octal-channel high-speed ADC, with up to 65 Msps sampling rate [10] was connected to a Xilinx SP601 evaluation platform, via an FMC connector provided on the board. Four channels of the ADC module were used in the current implementation. A Xilinx Spartan-6 FPGA is installed on the board, which contains a 128 MByte DDR2 component memory and a gigabit ethernet used in the current implementation [11]. A function generator was used to clock the ADC [12].

2.2. Acquisition method

2.2.1. Hardware description. Figures 1 and 2 illustrate the developed architecture. The Xilinx embedded development kit (EDK) [13] was used for the design. The system clock was 66.67 MHz for this platform.

The ADC has four low-level differential signaling (LVDS) outputs, each one providing to the FPGA a serial 12 bit data bitstream. An LVDS high-speed clock output and an LVDS delayed repowered sampling clock are also provided. The FPGA can receive LVDS data streams at the required speed without problems when the interface design is carefully constructed. A custom core written in VHSIC hardware description language (VHDL) was created for this purpose. Core's operation was verified using the ISim simulator by Xilinx. The core was connected directly to a memory controller (MPMC) [14] provided by Xilinx in order to achieve high data rate storage to the external memory and transmission to computer. The MPMC is also clocked at 66.67 MHz. The memory controller supports several types of interface ports. The most basic and high performance of these is the native port interface (NPI), which was chosen to stream the ADC data to the double data rate (DDR2) component memory in the current design. The NPI operation was tested using Chipscope software package from Xilinx [15]. This interface can support

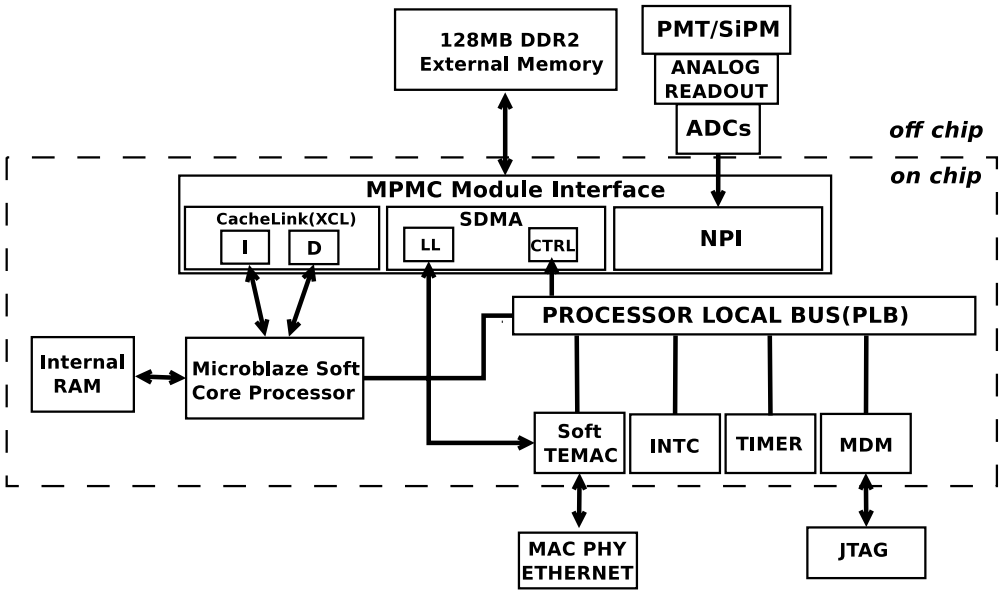


Figure 2. Block diagram of the acquisition front-end architecture.

bus widths of 32 or 64 bits. Due to the small size of the FPGA only the 32 bit interface could be used in the current design. The data rate with this interface was 2133 Mbps, fast enough to store the processed digitized data.

In the current design, the MPMC was configured to have two more ports. The Microblaze embedded processor [16] used the Xilinx CacheLink (XCL) port to access data and program stored in the DDR2 memory. The processor was used to control the transmission of digital outputs to a PC via ethernet. The ethernet controller [17] is connected to the soft direct memory access controller (SDMA) port of MPMC via a local-link interface.

The implemented system includes also the following EDK IP cores:

- a debug module (MDM) for online debug through the JTAG,
- an interrupt controller (INTC),
- a memory controller (EMC) for the internal memory of 8 KB.
- a timer.

2.2.2. Data collection. ADCs digitized data in the free running sampling mode [3]. The implementation uses the FPGA as a state machine. Before they are converted by the ADC, the detector signals are amplified and filtered by a low-pass filter to avoid aliasing. The digital outputs are continuously stored in four 16×12 bits shift registers for a sampling rate of 10 MHz when using the BGO scintillator and 30 MHz when using the LSO:Ce. Register's length depends on sampling frequency selection which is determined by the pulse width. A trigger signal was produced when the sum of the four ADC samples exceeded a given digital threshold, implying the arrival of an event. The state machine waits for a few clock cycles, whose number depends on pulse duration and ensures that the entire pulse will be stored. The integration of pulse samples for every channel ($\overline{X_a}$, $\overline{X_b}$, $\overline{Y_c}$, $\overline{Y_d}$) is calculated and the result is written to the DDR2 external memory. The calculation of the Cartesian coordinates x and y that correspond to the position of an event inside the FPGA was not possible due to the limited FPGA resources. For every 1000 events stored in the memory, an interrupt signal occurred. Microblaze was programmed in C language to read data from memory at every interrupt and to pass them to the LWIP networking stack [18], which was used for sending data to a server running on a linux machine, using the user datagram protocol (UDP). A timer was used to interrupt at a constant interval for sending the UDP datagrams. The data rate of the system can reach 60 Mbits s^{-1}.

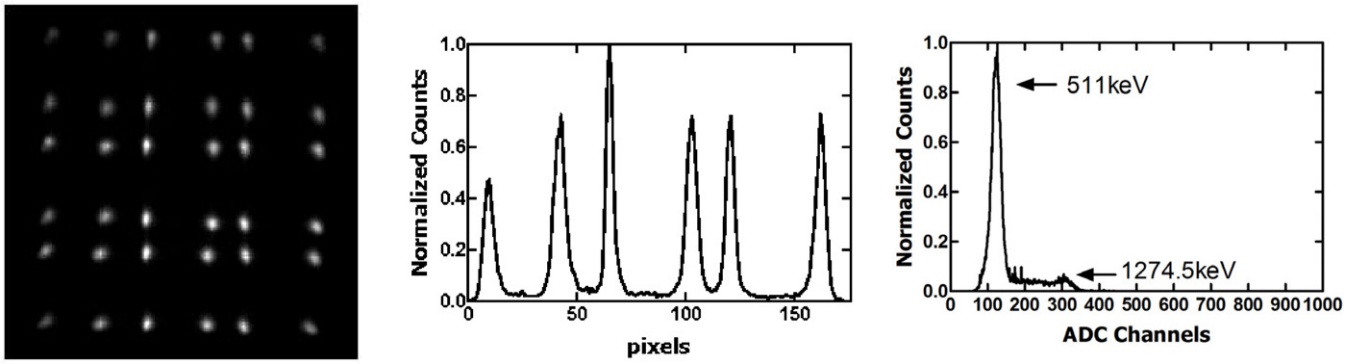
2.2.3. Postprocessing of digital outputs. The Cartesian coordinates x and y that correspond to the position of an event can be determined from the four outputs [19]:

$$x = \frac{\overline{X_a} - \overline{X_b}}{\overline{X_a} + \overline{X_b}}, \qquad y = \frac{\overline{Y_c} - \overline{Y_d}}{\overline{Y_c} + \overline{Y_d}}. \tag{1}$$

3. Results and discussion

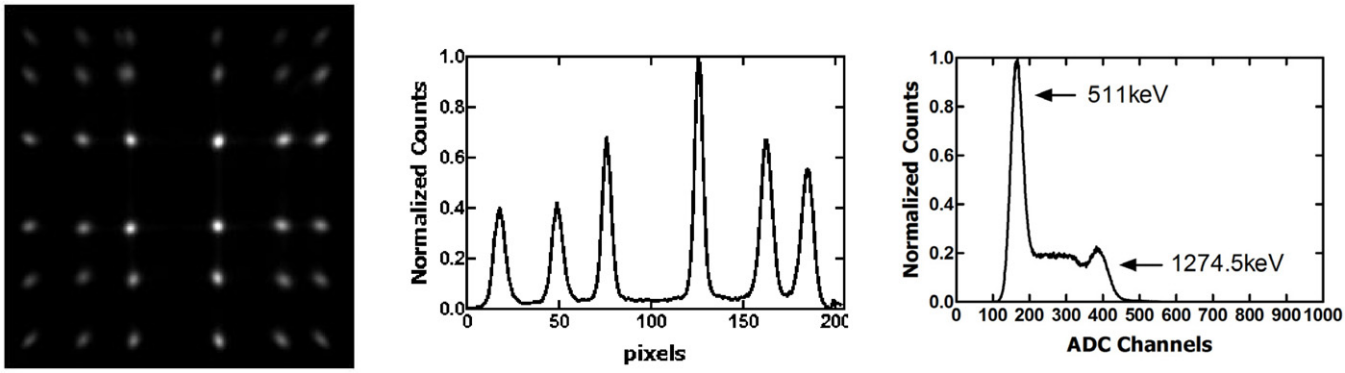
Figure 3 shows the results for the imaging gamma probe based on a Hamamatsu R8900U-00-C12 PSPMT coupled to a BGO scintillator array with a crystal element of size $2 \times 2 \times 5$ mm^3. The low pulse filter applied to the original detector pulse (500 ns in duration) in order to avoid aliasing has as a result a pulse rise time of 500 ns before digitization. The ADC sampling rate was chosen to be 10 MHz in order to collect 16 samples for a 1.4 μs pulse duration.

A 1 μCi ^{22}Na source was used in all experiments. The acquired flood map (figure 3(*a*)) and horizontal line profile (figure 3(*b*)) show a clear identification of all crystal elements.



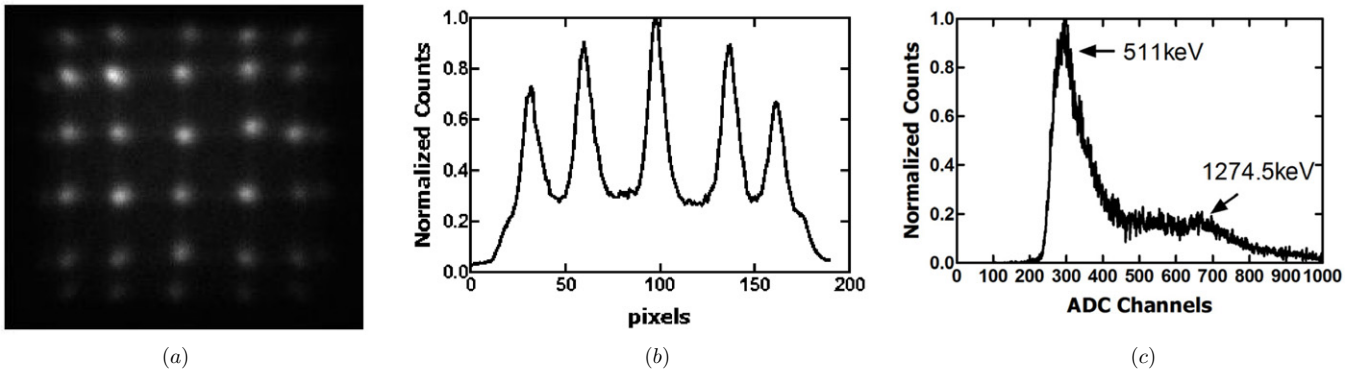
(*a*) (*b*) (*c*)

Figure 3. BGO coupled to a PSPMT excited with ^{22}Na: (*a*) flood map, (*b*) horizontal line profile and (*c*) energy spectrum of one central crystal element.



(*a*) (*b*) (*c*)

Figure 4. BGO coupled to SiPM excited with ^{22}Na: (*a*) flood map, (*b*) horizontal line profile and (*c*) energy spectrum of one central crystal element.



(*a*) (*b*) (*c*)

Figure 5. LSO:Ce coupled to a PSPMT excited with ^{22}Na: (*a*) flood map, (*b*) horizontal line profile and (*c*) energy spectrum of one central crystal element.

The average peak to valley ratio was 41:1. Figure 3(*c*) shows the energy spectrum of one crystal element. The mean energy resolution of all crystal elements was 26%.

Figure 4 shows the results for the imaging gamma probe based on a SensL's SiPM array coupled to the same BGO. Again a sampling frequency of 10 MHz was enough for the digitization of detector signals. A clear identification of the pixels was achieved (figures 4(*a*) and (*b*)). The average peak to valley ratio was 7.5:1. Figure 4(*c*) shows the energy spectrum of one crystal element. The mean energy resolution of all crystal elements was 25%.

The system provides accurate results in the case of fast LSO:Ce pulses. Figure 5 shows the results for the gamma probe based on SensL's SiPM array coupled to an LSO:Ce with $2 \times 2 \times 15$ mm^3 pixel size. Because of the intrinsic radioactivity of LSO:Ce, the final image was acquired from the subtraction of two images taken in the same duration: the first one was acquired with the radioactive source upon the detector and the

latter without this. Figures 5(*a*) and (*b*) show clear visualization of crystal elements. The average peak to valley ratio was 3.2:1. Figure 5(*c*) shows the energy spectrum of one crystal element. The mean energy resolution of all crystal elements was 24%. The ADC sampling frequency was chosen to be 30 MHz in order to collect 16 samples, for a 500 ns (100 ns rise time) pulse duration after the amplification stage.

4. Conclusions and future work

A four-channel FPGA-based data acquisition system has been successfully developed and tested with two different optical detectors for use in nuclear dedicated imagers. The use of FPGA along with high speed ADCs via the FMC connector increases flexibility and enables module reuse in different detectors. Digitized pulses were integrated inside the FPGA and transferred to a PC via an ethernet link. The calculation of the Cartesian coordinates x and y that correspond to the position of an event inside the FPGA was not possible due to the limited FPGA resources. At the moment, only four channels out of the eight channels available are used with the current FPGA, limiting the implementation to single-photon-detection applications. A new platform based on a different FPGA that provides more logic cells, along with the current octal-channel ADC board is under development. The available resources will be used for the implementation of digital signal processing filters, to extract the timing information of the detected scintillation pulses which is essential for the readout of PET detectors.

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