HRM-TDC Software Release Notes

Date	19th April 2012
Rev	3.0
File name	HRM-TDC_Install_3p00.exe
Reason for Change	Change to new “Active Installer”. GUI and drivers remain the same. Rev gone to 3.00 to keep in line with other products using the same new installer
Date	23rd September 2014
Rev	3.1
File name	HRM-TDC_Install_3p01.exe
Reason for Change	Change to include QuickUSB.h explicitly in the QuickUSB folder.
Date	29th October 2015
Rev	3.2
File name	HRM-TDC_Install_3p02.exe
Reason for Change	Change for new rev of FPGA. Now at 1.12

SOFTWARE REVISION HISTORY

SIE2 GUI

Date	Rev	Reason
6-Sep-2007	1.02	Frozen – No further development

HRMTime DLL Drivers

Date	Rev	Reason
6-Sep-2007	1.01	First release of code
5-Jul-2008	2.00	1. Add HRM_GetTimeTagGap function 2. Add HRM_GetLastError function and error reporting
3-Jun-2008	2.01	1. Add HRM_RunFifoTimeTagging function 2. Add HRM_GetTimeTagGap function 3. Add HRM_FixTimeTags function 4. Add HRM_GetMemorySize function
14-Nov-2008	2.02	1. Change code to allow RESYNC FIFO TimeTagging mode. Global variable ResyncTTAG is set for new mode if the FSR is set to 0xFFFF. 2. Change functios to accout for new Time-Tagging mode. 3. Fix HRM_RunFifoTimeTagging bug for resolutions other than 27ps.
14-Feb-2009	2.03	1. Change code to allow RESYNC FIFO TimeTagging mode to run with a 4us block rather than a 1us. 2. Add 'mode' parameter to FIFO functiions. 3. Add new function HRM_ConvertRAWtoCSV.
10-May-2010	2.04	Change 'ReadMemory' code to allow enable/disable of 6 channel smoothing.
18-April-2011	2.05	Change 'ReadMemory' free MALLOC memory. Was getting memory erosion.
26-Jun-2011	3.00	1. Remove FEATURES so license not required. 2. Make non-smoothing the default setting

File Names: HRMTimeAPI. DLL
HRMTimeAPI_LV.DLL

HRMTime FPGA Firmware

Date	Rev	Reason
25-Jan-2007	1.01	First release of code
25-Mar-2007	1.02	Change state machine to lengthen time for reading the TDC. Multi-channel readings were producing spurious results.
26-Apr-2007	1.03	1. Introduce 'Mgate' to latch MACRO times to changing data while writing time-tags to memory. -- 2. Replace I-MODE continuous time-tagging with R-MODE version plus free running MACRO counter to check for wrap-rounds.
22-May-2007	1.04	Add delay to ensure state of Mdone is clear from previous memory access.
18-Jun-2007	1.05	Synchronize state machine reset to clock. Found to make state machine more stable from reset.
11-Oct-2007	1.06	The HI-LO word clock (uwCLK) was glitching due to the possibility of USBREN and CMD_DATA changing at the same time. This caused some modules to lose the first word (2 bytes) of a USB block transfer. The clock is now gated with a delay version of CMD_DATA.
12-Nov-2007	1.07	The latching over of the next data from memory into the USB buffer was not always occurring. This caused two consecutive 32 bit words to occasionally be the same value. This appears to have been a metastability problem that latching, using bCLK, within the state machine fixes.
11-Nov-2008	1.08	1. Change to MARCO counters latching (to fix instability). 2. Use the RESYNC signal to set the mode of operation in FIFO Time-Tagging mode.
14-Feb-2009	1.09	RESYNC FIFO Time-Tagging problem due to fixed channel priority. The priority is now rotated as each event is detected.
30-Sep-2009	1.10	Priority was using a counter. This made it possible for a channel just hit to get highest priority next time. Now the priority states are specified.
11-May-2010	1.11	Create an Address Gating (ADGATE) output to create a READ-MODIFY-WRITE protection for histogramming. Without this the PIXEL and LINE counters can asynchronously change the address when the BIN is being incremented.
29-October-2015	1.12	Fix FIFO Time-tagging issue by removing FPGA compiler compression to configuration file.

File Names: HRMTime_1p12.pof
HRMTime_1p12.rpd

Note: FPGA upgrades should only be carried out if absolutely necessary. If an upgrade is deemed necessary, it should be carried out with SensL supervision.